STAGGER/DESTAGGER MODIFICATION FOR THE AIR TRAFFIC CONTROL RADAR BEACON SYSTEM

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National Aviation Facilities Experimental Center
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STAGGER/DESTAGGER MODIFICATIONS FOR THE AIR TRAFFIC CONTROL RADAR BEACON SYSTEM

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JANUARY 1976

FINAL REPORT

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16. Abstract

The air traffic control radar beacon system (ATCRBS) was modified so as to eliminate false or second-time-around aircraft replies. A dual-channel stand-alone modification equipment unit was developed to stagger the beacon interrogations and destagger the reply video. The unit can be used with any beacon interrogator defruiter or processor. Two models, an analog and a digital, were developed. The resulting equipments were implemented and tested at the Bedford, Virginia, long-range radar facility.

During the engineering tests and operational evaluation, the stagger modification performed reliably. It is recommended that the digital version be implemented at the field facilities.

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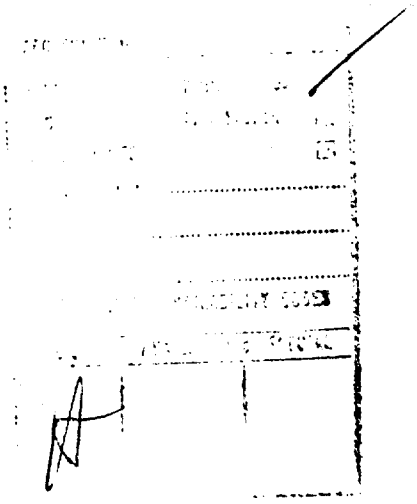

INTRODUCTION

PURPOSE.

The objective of the project effort was to develop a modification for the ground interrogator-receiver system which would allow the associated video processing equipment to remove second-time-around targets from the system.

BACKGROUND.

In the operation of an air traffic control beacon system, it is common to receive false radar beacon replies due to a phenomenon referred to as "second-time-around" targets. Second-time-around targets occur when an aircraft is beyond the set operating range of a ground interrogator-receiver-display system, but does reply despite its long distance. A condition then exists whereby a distant aircraft transponder reply to one interrogation is received and processed during the receive time associated with the following interrogations. A group of replies associated with one scan of the ground interrogator-receiver antenna across a target aircraft thus produces a false target at a pseudo range, usually close-in to the radar site, to the obvious detriment of the system.

DISCUSSION

THEORETICAL CONSIDERATIONS.

Target replies which appear synchronous, i.e., have an essentially constant time relationship with a master timing source over several interrogation periods, are processed as valid targets. Replies which appear asynchronous are discarded. The purpose of stagger/destagger is to make second-time-around targets appear asynchronous.

Stagger/destagger is implemented by incorporating a center-tapped delay line in both the interrogator trigger path and the reply video path. The exact electrical length of the delay line is a function of the range cell resolution and range comparison criteria of the automated processing equipment. The center tap of the delay line must be within 25 nanoseconds (ns) of the true electrical center over the normal operating temperature range of the device. Center-tapped delay lines of 7.6 microseconds (μs) and 7.2 μs were used in the two types of stagger/destagger equipment designed, fabricated, and tested.

In the conventional beacon system, a master timing trigger signal, referred to as the beacon sync signal, recurs at a precisely fixed interval. The interval varies from system to system to minimize interference, but will generally be approximately a 3,000-μs interval. Beacon interrogator mode trigger signals

are generated from beacon sync signals after a fixed delay. The delay is adjustable to allow range coincidence between beacon targets and targets from an associated radar, but once the proper delay is determined, it remains constant. Figure 1a shows the basic timing of a beacon system.

As the beacon antenna scans across a target, a series of replies will be generated by the aircraft transponder and received at the interrogator site. Ideally, one reply will be received for each interrogation. Each reply from a given target will have essentially the same time (range) measurement from beacon sync (range zero). Operational criteria establish target detection based on a given number of equal-range replies within a given number of consecutive interrogator-reply cycles.

The stagger/destagger system is implemented by inserting a center-tapped delay line in the trigger-generating path and in the video reply path. The delay line can be inserted anywhere in the system between the trigger (beacon sync) generator and the interrogator. In the equipments under discussion, the delay line was inserted after the mode trigger generator as shown in figure 1d. By switching delay line taps at the beginning of each interrogate period, the interrogator triggering is caused to shift with respect to beacon sync. When the interrogator triggering is shifted, the reply video will also shift unless compensated for by inserting an equal and opposite delay in the reply video path.

Figures 1a, 1b, and 1c show the three positions which the interrogator triggers may assume with respect to beacon sync in the stagger system. The dashed target reply in figure 1b and 1c shows where the reply video would fall if not compensated by an equal and opposite delay (destaggered).

The amount of destagger delay required in the video path is precisely equal but opposite to the amount of stagger delay inserted in the trigger path; thus, it is obviously desirable to use the same delay line for both functions (figure 1e). However, since the delays must be in opposite directions, a switching system is required both to select the appropriate delay line taps and to differentiate between trigger processing and video processing. There is no adverse effect on system operation if staggered trigger pulses appear on the destaggered video output line but the reverse is not true; therefore, reply video must be inhibited from the stagger/destagger delay line during trigger processing time. This will normally be taken care of automatically by the receiver sensitivity time control (STC) and/or gated time control (GTC), which cuts off the receiver for a period of time extending from shortly before beacon sync until zero range. If the receiver does not have STC/GTC provisions, the switching system must be designed to provide the necessary video inhibiting.

Assuming that the timing relationship of an unmodified system is as shown in figure 1a, then, when the stagger/destagger is incorporated, the original fixed delay between beacon sync and mode triggers is reduced by an amount equal to the length of the stagger delay line. Insertion of the stagger delay line now returns the system to its original timing configuration provided the triggers are processed from the output tap of the stagger delay line and the video is processed from the input tap of the stagger delay line. This is

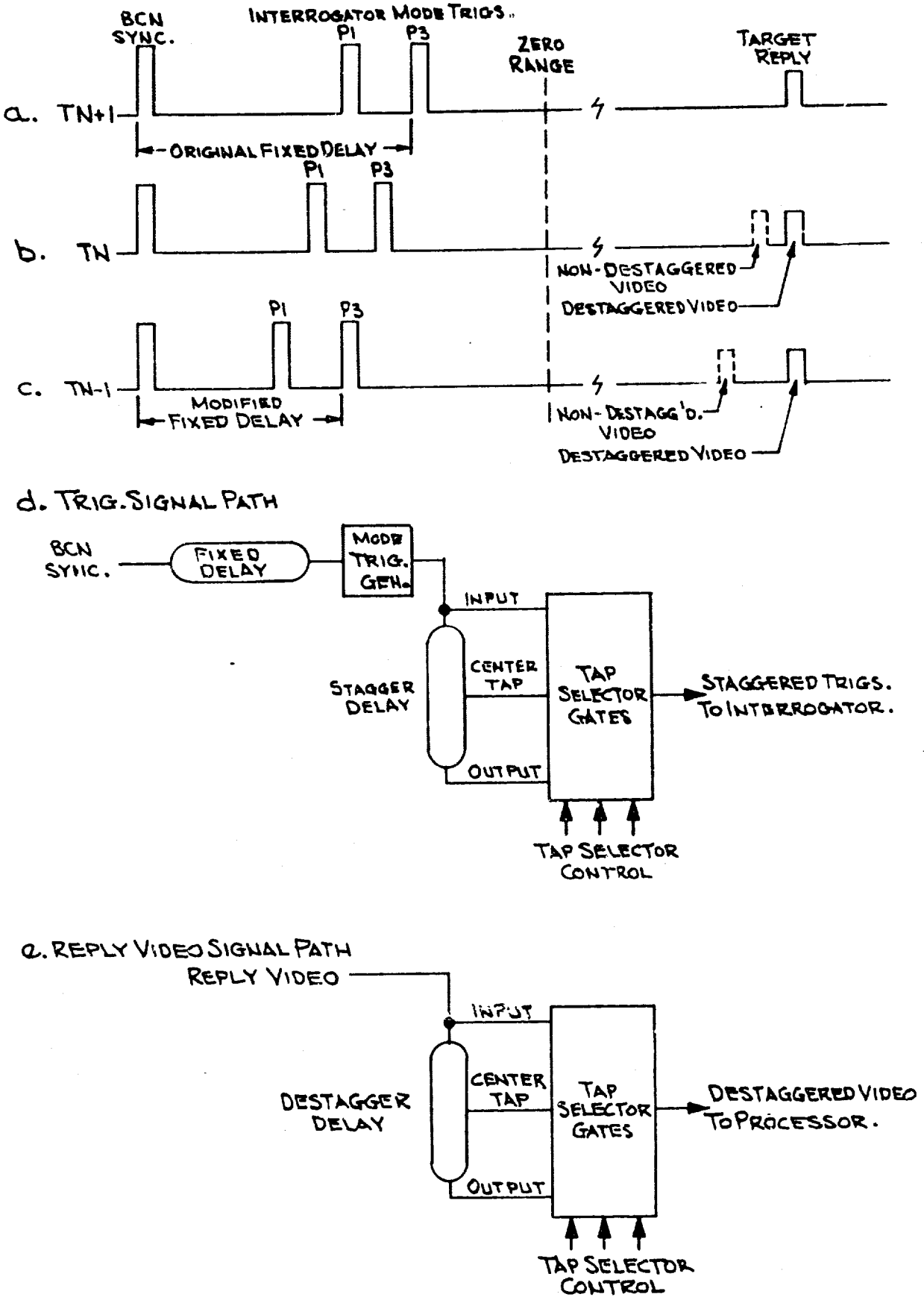

FIGURE 1. STAGGER/D!'STAGGER TIMING AND PATH DIAGRAMS

the standard configuration for nonstaggered operation when the stagger modification is installed. When staggered operation is implemented, trigger processing is switched among the three delay line positions, once per interrogation period, in a predetermined sequence. Switching of delay line taps is accomplished coincident with the first trigger (i.e., with beacon sync or P_1). With each delay line configuration for trigger processing, there is a corresponding configuration for video processing. When triggers are processed from the output tap (maximum delay), video is processed from the input tap, i.e., zero delay. When triggers are processed from the center tap, video is also processed from the center tap; and when triggers are processed from the input tap, video is processed from the output tap. Under these conditions, reply video from a discrete target within the set operating range of the system will appear at a constant range over successive interrogation periods.

The three conditions of trigger/video delay in stagger/destagger operation are designated as TN+1, TN, and TN-1. The delay line taps from which trigger and video are processed for each condition are shown in table 1.

The theory of operation of stagger/destagger can readily be perceived by means of the chart constituting table 2. The interrogator triggers can assume any one of three time slots with respect to beacon sync. These slots are designated as 1, 2, and 3 in table 2 and correspond to trigger processing from the input, center, and output taps of the stagger delay line, respectively. Immediately below the slot designations are the corresponding stagger/destagger designations (TN-1, TN, TN+1) as described in the previous paragraph. Each horizontal line in table 2 represents one interrogation/reply cycle. X1 indicates that the interrogation in the first cycle occurred in time slot No. 1 (TN-1). The reply from the target of interest will arrive back at the receiver in the corresponding receive time slot as indicated by R1. In the TN-1 configuration, the reply is delayed two time slots (the full length of the destagger delay line) by the destagger delay. The reply therefore arrives at the video processing equipment during receive time slot three, as indicated by R1(D).

The second interrogate cycle (X2) is shown occurring in the third time slot. The reply (R2) will therefore arrive in receive time slot No. 3. Since this is the TN+1 condition, the reply video will not be delayed, and the video will arrive at the processing equipment at receive time No. 3.

The fourth interrogate cycle (X4) is shown occurring in the second time slot. The reply video will therefore arrive in the second receive time slot. Since this is the TN condition, the video will be delayed one time slot before being sent to the video processing equipment.

From table 2a, it is readily apparent that, regardless of the time slot in which the interrogation occurs, the reply video will always arrive at the processing equipment at receive time No. 3, thereby satisfying the prime requisite for target recognition.

TABLE 1. DELAY LINE TAPS PER STAGGER CONDITION

Condition	Delay Line Tap	
	Trigger	Video
TN+1	Output	Input
TN	Center Tap	Center Tap
TN-1	Input	Output

TABLE 2. TRANSMIT AND RECEIVE TIMES FOR VALID AND SECOND-TIME-AROUND TARGETS

a. Valid Targets

	Transmit Time Slots			Receive Time Slots				
Interrogate/Reply Sequence	1 (TN-1)	2 (TN)	3 (TN+i)	1	2	3	4	5
1	X1			R1		R1(D)		
2			X2			R2 R2(D)		
3	X3			R3		R3(D)		
4		X4			R4	R4(D)		
5		X5			R5	R5(D)		
6	X6			R6		R6(D)		

b. Second-Time-Around Targets

1	X1							
2			X2	R1				
				R1(D)				
3	X3					R2		R2(D)
4		X4		R3	R3(D)			
5		X5			R4	R4(D)		
6	X6				R5		R5(D)	

NOTE: X = Transmit
R = Receive
D = Delayed

Table 2b shows the timing relationships for second-time-around targets. The first reply (R1) is shown occurring in the first receive time slot of the second interrogate/reply cycle. The reply was actually generated by the first interrogate cycle, but did not arrive at the receiver until after the second cycle had been initiated. Since the system is in the TN+1 condition upon receipt of the reply, there is no delay between the receiver output and the input to the video processing equipment, and thus it remains in receive time slot No. 1. Likewise, reply R2 is received during the third interrogate/reply cycle. It occurs during the third receive time slot, since it was generated by X2 in the third time slot. Since the system is in TN-1 condition when R2 is received, the video is delayed two additional time slots. Following through the complete series of interrogations it will be seen that no two consecutive second-time-around replies appear at the video processing equipment in the same time slot, thus target detection criteria are not met.

The stagger pattern is specifically chosen to produce the condition shown in table 2b. The pattern is TN-1, TN+1, TN-1, TN, TN and is repetitive as long as the system is in staggered operation. From the foregoing discussion, it is obvious that a second-time-around target will recur in the same time slot or range cell only every fifth interrogation when the stagger modification is used. The stagger/destagger modification equipment contains provisions for nonstaggered operation in which case the system is locked in the TN+1 condition.

EQUIPMENT CONFIGURATION.

Two types of stagger/destagger equipments were designed, built, and tested. The first type processed the video in analog form, thus requiring linear amplifiers throughout the video circuitry. Theory of operation and diagrams for this system are contained in appendix A. For the second type, a two-level quantizer was incorporated in the video input circuitry, and all processing from the quantizer through the remainder of the system used digital techniques. The theory of operation and diagrams for this system are contained in appendix B.

TESTS AND RESULTS

The first system, employing analog video processing, was tested operationally at the FAA enroute radar site at Bedford Air Force Station, Virginia, for a period of approximately 4 months. The second system, employing digital video processing, was installed at the same location, replacing the analog system, and has been in operation for approximately 2 1/2 months.

Except for a premature power supply failure in the analog system, both systems have provided satisfactory service and have accomplished the desired objective. Second-time-around targets have been removed from the beacon radar displays with no degradation to system performance.

CONCLUSION

Incorporation of a stagger/destagger modification kit is technically feasible and operationally desirable at locations experiencing problems with second-time-around beacon targets.

RECOMMENDATION

It is recommended that the digital-type stagger/destagger modification for the ATCRBS system be adopted. The digital version is more reliable and less expensive, since it requires fewer components and adjustments to accomplish the desired results.

APPENDIX A

ANALOG STAGGER EQUIPMENT MOLIFICATION

STAGGER/DESTAGGER MODIFICATION

Project 031-241-070

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LIST OF ILLUSTRATIONS

1. INTRODUCTION.

1.1 FUNCTIONAL DESCRIPTION. In a nonstaggered system, the second-time-around replies appear as synchronous targets at pseudo ranges. It thus becomes necessary to cancel these false targets. This is effected by a staggering of successive interrogations. This is accomplished by staggering the pulse repetition times (PRT's) or the mode triggers and then destaggering the video replies as necessary, so that first-time-around synchronous targets remain synchronous and within proper time perspectives. Video replies are considered synchronous if they appear at times that have the proper relationships to the respective interrogation pulses. Second-time-around targets can appear synchronous if they appear at times that have the proper relationships to the respective interrogation pulses. A second-time-around target can appear synchronous in the following manner: Assume that interrogations occur every 2,000 microseconds (μs), and there is a target at 2,500μs; in response to the first interrogation, the first reply occurs 500μs after the second interrogation. The second reply, in response to the second interrogation (which occurred at 2,000μs), is received 500μs after the third interrogation, which is 2,500μs after the second interrogation. Since these replies each occur at 500μs following an interrogation, normal reply processing equipment will consider them synchronous. It is the function of the stagger/destagger modification to cancel these pseudo second-time-around targets, while maintaining the timing of real targets in the proper time perspectives.

1.2 TIMING CONSIDERATIONS. Consider the following:

TN+1 = an occurrence at beacon sync plus a fixed delay.

TN = an occurrence 3.8μs prior to TN+1.

TN-1 = an occurrence at 7.6μs prior to TN+1.

When interrogation transmissions occur at TN-1, the received video is delayed by 7.6μs. When transmissions occur at TN, the received video is delayed by 3.8μs. When transmissions occur at TN+1, the received video is not delayed. With proper sequencing in transmitting pulses at TN-1, TN, and TN+1, second-time-around targets are forced to assume a nonsynchronous position in relation to destaggered P_3. In the scheme, this enforced relationship will hold for any two consecutive interrogations in any given mode. Further, for any 11 consecutive interrogations in a given mode, no more than three second-time-around targets will appear to be at a single, discrete range with respect to destaggered P_3. This is in accordance with the validation criteria of the common digitizer.

The interrogation transmission sequence is:

TN-1, TN+1, TN-1, TN, TN.

This transmission staggering cycle is effective for all interlace patterns when the interrogator is operated in conjunction with video defruiting or common digitizing equipment.

The stagger/destagger logic shown in the National Aviation Facilities Experimental Center (NAFEC) drawing XD-2706 accomplishes this precise stagger/destagger scheme. (See 6. STAGGER/DESTAGGER SCHEMATICS.)

The video destaggering process consists of introducing the proper delay, by means of logic gates and a lumped constant delay line, to the received video pulse train so that total stagger/destagger delay is a constant 7.6 $\pm$.025μs.

1.3 DELAY LINE. A sirgle delay line (DL) is used to provide the delays for the staggering as well as the destaggering process. The characteristics of the DL that are important include a temperature coefficient which is consistent with the delay accuracy requirement of 7.6 $\pm$.025μs, and a delay-to-rise-time ratio that will not degrade video pulses having the following typical characteristics:

Rise time:	0.1μs
Decay time:	0.2μs
Slope:	2 percent

A block diagram of the stagger/destagger modification is shown in NAFEC drawing XD-2707.

2. THEORY OF OPERATION.

2.1 CONTROL LOGIC.

2.1.1 General. The stagger/destagger control logic is a group of transistor-transistor logic (TTL) plug-in modules assembled and wired on a universal integrated circuit (IC) packaging board. The functions of the control logic are to:

a. Generate stagger pattern sequence,
b. Provide switching between trigger and video processing,
c. Delay the source trigger to the analog circuitry, and
d. Provide synchronizing triggers for test equipment.

(Refer to block diagram drawing XD-2707)

A 7.6μs delay line with taps at zero, 3.8, and 7.6μs provides the necessary delays to stagger the trigger and destagger the video. The zero delay tap is designated "TN-1 tap," the 3.8μs tap is designated "TN tap," and the 7.6μs tap is designated "TN+1 tap."

In the nonstagger (STAGGER) mode of operation the trigger is gated from the TN+1 tap (i.e., delayed 7.6μs from the source) and video is gated from the TN-1 tap (i.e., zero delay). In the stagger mode of operation, successive triggers are gated from the various taps in the following repetitive sequence: TN-1, TN+1, TN-1, TN, TN. When the trigger is gated from a delay line tap earlier than 7.6μs, the video associated with that trigger must be delayed a comparable amount in order for a target to appear at the correct range. It is important to remember that the trigger delay plus the video delay must equal 7.6μs. The selection of the appropriate DL tap is accomplished by the control signals from the pattern generator. The control signals are labeled TN, TN-1, and TN+1, to correspond with the pattern terminology, and are postscripted with a (T) or (V) to differentiate between trigger control and video control. Thus, the TN+1 (T) control signal enables trigger processing from the TN+1 tap (7.6μs) and the TN+1 (V) control signal enables video processing from the TN-1 tap (zero). The TN-1 (T) control signal enables trigger processing from the TN-1 tap (zero) of the DL, and the TN-1 (V) control signal enables video processing from the TN+1 tap (7.6μs). During TN time, both trigger and video are enabled from the TN tap (3.8μs) of the DL.

The control signals representing the pattern, TN-1, TN+1, TN-1, TN, TN are derived from a modified divide-by-five counter and associated gates. The The divide-by-five counter is incremented once per interrogation period by the source trigger. The pattern control signals for switching the video processing to various taps of the delay line are obtained directly from the output gating of the divide-by-five counter, but must be modified for trigger switching so as to be "high," only during the period from the leading edge of the first source trigger "in" to the trailing edge of the last staggered trigger "out." This is accomplished by the data selector.

2.1.2 Detailed Logic Description. (Refer to NAFEC drawing XD-2706.)

The pattern generator is comprised of a divide-by-five counter consisting of three flip-flops (C3B, C2B, C2E) and associated gates located in zones C2 and C3. When the stagger switch S2 is in the nonstagger (STAGGER) position, the three flip-flops are held in a steady state, resulting in the TN+1 signal being high. When the stagger switch is in the stagger (STAGGER) position, the divide-by-five counter is toggled by the stagger clock and generates a recurring pattern of TN-1, TN+1, TN-1, TN, TN.

The synchronizing triggers for test equipment are generated from flip-flop C2B of the divide-by-five counter. Flip-flop C2B is in the "one" state for three interrogation periods and in the "zero" state for two interrogation periods during staggered operation; therefore, either of its outputs may be used to generate a positive or negative transition, once per pattern. This results in the 1P output. The output of flip-flop C2B is fed simultaneously to a divide-by-three counter (BIE and BIF) and a divide-by-four counter (BIC and BID) resulting in the 3P and 4P outputs. The 1P, 3P, and 4P outputs are incorporated in the equipment to facilitate testing with various interlace ratios.

The six type 74L00 logic gates (B2B through B2G) connected in series from the junction of divider networks R1 and R2 are used to delay the source trigger to the DL approximately 120 nanoseconds (ns). The purpose of this delay is to allow the pattern generator and control logic to assume a new state upon receipt of a source trigger prior to the source trigger reaching the DL.

The function of the remaining logic on drawing XD-2706 is to generate one stagger clock pulse per PRT regardless of whether the source trigger is a single pulse or multiple pulses and to provide a staggered output pulse for triggering a test set during routine system checks.

An 8-volt to 70-volt source trigger is fed to a 7413 Schmitt trigger (B3A) via divider network R1, R2. Schmitt trigger B3A inverts the source trigger and converts it to TTL logic levels. The output of B3A is the "stagger clock" to the divide-by-five counter. The Schmitt trigger output also triggers a single-shot multivibrator (B3B) whose $\overline{Q}$ output "sets" flip/flop (F/F) A2C thus removing the "direct reset" to F/F B1A and allowing it to be "set" by the trailing edge of the inverted stagger clock.

The trigger occurring at B2G is delayed approximately 120 ns from the input trigger and is then processed through the DL circuitry. The staggered trigger output of the DL circuitry will be delayed zero, 3.8, or 7.6μs depending on which control signal from the divide-by-five circuitry is high. The staggered trigger output will be either a single pulse or multiple pulse depending on the trigger source.

The staggered logic circuitry located in zone A consists of a resistive divider network, two inverters, a single-shot multivibrator (MV), a bistable MV, a down counter, and a count selector switch. Staggered triggers are reduced to TTL logic level by the resistive divider consisting of R3 and R4. The leading edge of the first pulse triggers the single-shot A3B into its unstable state for approximately 180μs. While the single-shot A3B is in its unstable state, down counter A2A will decrement one count on the trailing edge of each trigger pulse. When the down counter reaches zero, the next pulse causes an output pulse to be generated, the trailing edge of which resets F/F A2C. The down counter is preset to a particular count by means of the associated hexadecimal switch A2E, which is mounted in a dual-in-line package on the logic board. Whenever the single-shot (A3B) is in its stable state, the count of the hexadecimal switch is automatically loaded into the down counter. The preset count must equal one less than the number of trigger pulses expected per interrogation period.

Flip-flop A2C is used to enable the staggered trigger circuitry only during the trigger generating portion of an interrogation period. The "set" output of F/F A2C goes high on the leading edge of the first source trigger of the interrogation period through the action of single-shot B3B, and goes low on the trailing edge of the last staggered trigger of the interrogation period through the action of the down counter A2A and inverter A2B. The "set" output of F/F A2C is "anded" with the pattern signal in the data-selector module C1A to produce the appropriate (T) pattern signal only during the trigger generating period.

The ripple clock output of the down counter A2A is inverted by gate A2D and fed to a discrete component trigger amplifier. The ripple clock output is a single pulse per interrogation period. The trigger amplifier increases the amplitude of the ripple clock from TTL level to approximately a 30-volt (V) pulse. The output of the ripple clock is fed to J5 for use with external equipment.

2.2 ANALOG CIRCUITRY. (Refer to block diagram NAFEC drawing XD-2707.)

2.2.1 General. The analog portion of the system consists of three identical amplifier/switch (A/S) cards, an input/output (I/O) card, and a DL.

Triggers and video are received by the I/O card, "OR'd," amplified, and fed to the DL.

The DL input tap, center tap, and end tap each feed an amplifier/switch card. The amplifiers on these cards restore the video so that it is equal to that of the incoming video. The amplifier outputs are then distributed to analog switches on the A/S cards and digital gates on the I/O card for video and trigger selection respectively.

The analog switch outputs are tied together at the output-video amplifier input. The selected video is then available at the video output.

The trigger-selection circuits receive inputs from the three DL taps. An enable on the trigger-select line (for the desired tap) gates the triggers to the output amplifier, where they are amplified to the 30-V level for distribution. (If the enable line is high during video time, video will also be present at the trigger output as 30-V triggers.)

2.2.2 Input/Output Amplifier. (Refer to NAFEC drawing XD-2701.)

2.2.2.1 Input Amplifier. The video input is buffered by emitter followers Q1 and Q3. Q4 and Q5, with associated components, form a noninverting amplifier with a gain of approximately four. A gain of approximately two is required as one-half the signal is lost via the DL input terminating resistor R24. Gain is controlled by attenuating the input to the fixed gain amplifier Q4 and Q5 by adjustment of gain control R11.

Video is inhibited during the trigger generating period by the action of three gates in 7403 IC module U2. Whenever TN (T), TN-1 (T), or TN+1 (T) is high, the common output of the three gates is low. This clamps the input to Q3 at approximately zero volts and prevents any video from reaching the DL.

When a trigger is received from the 120-ns DL in the control logic, the output of the remaining gate in U2 goes low, turning ON Q2, which produces approximately 4 V across the gain control R11.

The video and triggers are now coupled via C6 to the DL driver U1.

2.2.2.2 Output Amplifier. The input to U3 is the selected video from an amplifier/switch card. (The outputs of the three amplifier/switch cards are tied together at this point.) U3 is an integrated complimentary emitter-follower.

2.2.2.3 Trigger Output Amplifier. Trigger selection for the output is made via U4. Inputs to DL zero tap, DL 3.8 tap, and DL 7.6 tap are received from the appropriate amplifier/switch card. These signals are combined video and triggers. The trigger-enable signals TN-1 (T), TN (T), and TN+1 (T), must be high only during the desired trigger time, as any signal present during this gate time will be made into a trigger. At trigger time, the base of Q6 goes negative turning OFF Q6 which turns ON Q8 as the bases of Q7 and Q8 are biased to approximately 2 V. Q7 turns OFF Q9, and Q10 is turned ON via Q8. The voltage at the collectors of Q9 and Q10 goes to approximately +14 V. The trigger output goes to approximately 28 V. At the end of trigger time, Q6 is turned back ON, forcing Q7 and Q9 ON, Q8 and Q10 OFF, and the trigger output back to zero V. (The collectors of Q9 and Q10 are now at approximately -14 V.)

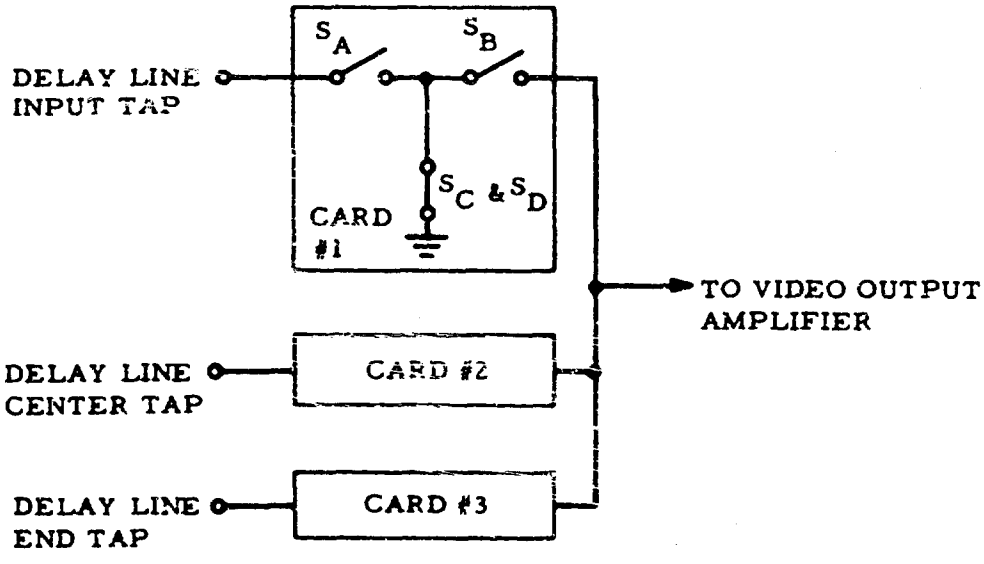
2.2.3 Amplifier/Switch Card. (Refer to NAFEC drawing XD-2700.)

The system contains three of these cards. All are identical so that only one will be described.

The input-video buffer U1 prevents loading of the DL tap This buffer drives an amplifier identical to that on the input card. The gain is adjustable from zero to four.

Switching of video is accomplished via U4, a COS/MOS integrated circuit. When the control lines are equal to V_{CC} the switches are closed. When the control lines are low, the switches are open.

In these cards, the switches are configured in the following manner:



When video from a particular tap is not selected, the two switches in series with it (SA and SB) are OFF, and the shunt switches (SC and SD) are ON to prevent crosstalk from one to the other. The switch control signals are timed so that the switches go ON slow and OFF fast.

If the video control input to the card is low, the control input to the series switches (U4-13 and U4-5) are low, and the switches are OFF (video is not selected). The control inputs of the shunt switches (U4-12 and U4-6) are high (approximately +10 V) and the shunt switches are ON. When the video control input goes high, U3-12 discharges C10, and the shunt switch control input goes low. C9 must be charged by R15 before the series control can go high, turning ON the series switches. This delay should be approximately 1μs (not critical). When the video control input goes low, C9 is discharged by the TTL input circuit so the series control goes low before the shunt control goes high, as R18 must charge C10 before the control input can go high.

2.2.4 Test Trigger Amplifier Card. The test trigger amplifier provides a 25-V trigger across a 75-ohm load from J5 on the rear panel of the chassis. The purpose of this output is to provide a staggered P_3 pulse for use during maintenance and testing.

The trigger amplifier is built up on a small printed circuit board which is mounted on an eight-pin adapter and plugged into the front left-hand corner of the logic board.

The schematic of the trigger amplifier is shown on NAFEC drawing XD-2709.

In the quiescent state, Q1 and Q2 are conducting and Q3 is cut off. This condition places -15 V on the negative side of the output capacitor.

When a trigger is received, Q1 is cut off, Q2 is cut off, and Q3 conducts, placing +15 V on the negative side of the output capacitor. The 30-V change from -15 to +15 on the negative side of the capacitor appears as a zero to +30 V change on the plus side of the capacitor.

2.3 INPUT/OUTPUT SWITCHING. The input to the STAGGER/DESTAGGER unit consists of source triggers and staggered video. The primary outputs are staggered triggers and destaggered video.

The inputs are routed through a coaxial switch so that in event of power failure or if the power switch is shut OFF, the inputs will be directly connected to the output jacks.

In normal operation, the input trigger and video signals are terminated with 75-ohm resistors mounted on the terminal strip on the back panel of the chassis. Ground for the terminating resistors is completed through contacts in plug/jack (P/J) 106 and through contacts on the front panel power switch. When the power switch is OFF, ground for the terminating resistors is open, and termination is provided at the end equipment.

P/J 106, located adjacent to power supply (PS)-2, is provided so that trouble-shooting can be performed on the STAGGER/DESTAGGER circuitry while the input signals are by-passing the unit. Separating the P/J 106 connection opens the 115 V alternating current (a.c.) line to the coaxial switch solenoid and breaks the ground to the input terminating resistors. Thus the power switch can be turned ON to provide operating voltages without double-terminating the input lines.

2.4 AUXILIARY OUTPUTS. The upper row of rear panel BNC jacks (J1 - J4) are the video and trigger input and output jacks. The lower row (J5 - J8) provides outputs for test and maintenance. J5 provides a staggered pulse output of approximately 25 V across the 75 ohms. This pulse is intended for use with a video generator or as a beacon test trigger to the common digitizer (CD).

J6, J7, and J8 provide 4P, 3P, and 1P synchronizing outputs intended primarily for triggering an oscilloscope. The 1P consists of one positive transition and one negative transition per stagger pattern. The positive transition occurs at the first TN-1 mode of the pattern.

The 3P and 4P synchronizing outputs provide similar transitions once every three patterns and once every four patterns respectively and may be useful for testing during various interlace conditions.

3. INSTALLATION.

The STAGGER/DESTAGGER modification chassis is provided with rack slides for mounting in any conveniently available 19-inch rack. Interconnection with the existing site equipment consists of providing a source of 115 V a.c., 60-hertz (Hz) power and making five video/trigger connections through BNC connectors on the rear panel of the chassis. The connections are:

- Trigger in (J1),
- Video in (J2),
- Destaggered video out (J3),
- Staggered trigger out (J4), and
- Test trigger out (J5).

These connections are illustrated in figure 3.1.

4. CHECKS AND ADJUSTMENTS .

4.1 STAGGER/DESTAGGER INITIAL CHECKS. The initial checks are:

Step 1. With power OFF, apply triggers and video.

Step 2. Check triggers and video at input and output jacks.

Step 3. Set the hexadecimal switch on the logic board for a count of one less than the number of mode interrogation pulses.

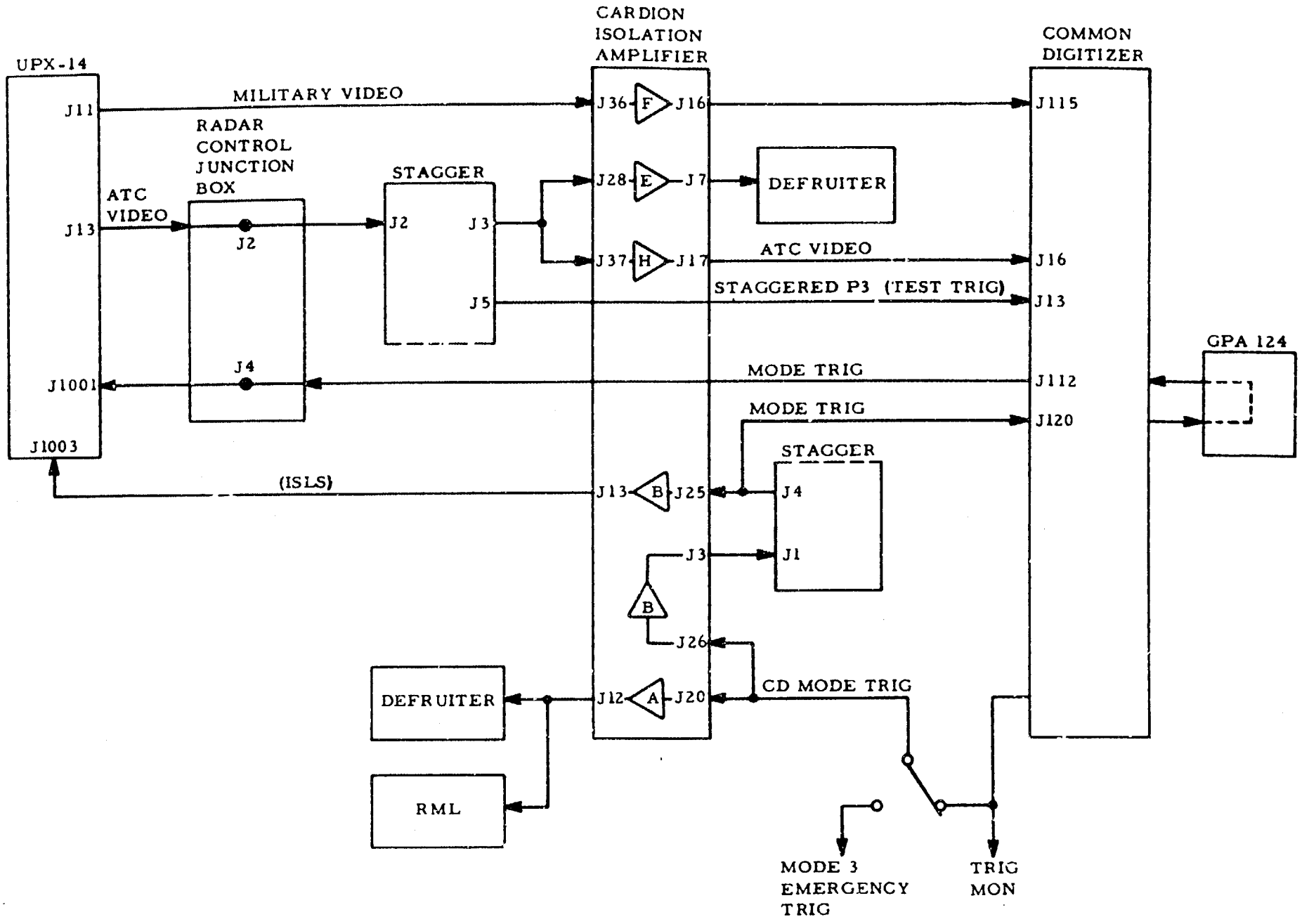


FIGURE 3.1. STAGGER/DESTAGGER INTERCONNECTION

Step 4. Apply power.

Step 5. With STAG/$\overline{\text{STAG}}$ front panel switch in $\overline{\text{STAG}}$ position, check for triggers and video at output jacks.

Step 6. Check for test trigger output at J5.

Step 7. Place STAG/$\overline{\text{STAG}}$ switch in STAG position.

Step 8. With oscilloscope triggered by beacon sync, and sweep set to less than one PRT, check test trigger output at J5. Three trigger pulses with baseline breakthrough should be observed. The triggers should be evenly spaced over an interval of 7.6μs.

Step 9. If checks do not produce expected results, refer to section 5.

4.2 STAGGER/DESTAGGER ADJUSTMENTS.

4.2.1 Input/Output Card Adjustment.

Step 1. Apply a 2-V video test signal to the video input jack (J2).

Step 2. Apply oscilloscope probe to the input tap of the delay line.

Step 3. Adjust R11 (potentiometer located on top edge of I/O card in J105) for 2-V video signal at input tap to delay line.

4.2.2 Amplifier/Switch Card Adjustment.

Step 1. Apply receiver video to video input jack (J2).

Step 2. Apply noninterlace mode triggers to trigger input (J1).

Step 3. Place front panel switch in STAG.

Step 4. Synchronize the oscilloscope with the 1P signal from J8.

Step 5. Observe output video at J3.

NOTE: The 1P signal is a positive transition once per stagger pattern (five PRT's). The pattern will be displayed on the oscilloscope in the order TN-1, TN+1, TN-1, TN, TN.

Step 6. Identify the TN+1 portion of the displayed pattern and adjust R1 of AMPLIFIER/SWITCH No. 1 (potentiometer located on top edge of card is J101) for 0.45 V of noise.

Step 7. Identify a TN portion of the displayed pattern and adjust R1 on A/S No. 2 (J102) for 0.45 V noise.

Step 8. Identify a TN-1 portion of the displayed pattern and adjust R1 on A/S No. 3 (J103) for 0.45 V noise.

4.3 COMMON DIGITIZER (CD) ADJUSTMENT. The CD timing must be changed to compensate for the 7.6-μs lumped constant delay and miscellaneous circuit delays added to the trigger path by the STAG/DESTAG modification. A coarse timing correction is made with the beacon pretrigger thumbwheels in the National Airspace System (NAS) interface equipment rack. This correction is in 0.1-mile (approximately 1.2-μs) increments. Final correction is made by restrapping card jumper wires on the CD. A change must also be incorporated to allow use of an external beacon test trigger.

Step 1. Set up coarse timing correction using thumbwheels o NAS interface equipment.

Step 2. Rejumper CD card CBFF6 to permit use of an external beacon test trigger.

a. Remove wire strap from 32 to 44.
b. Install wire strap from 32 to 19.

Step 3. Rejumper or install new cards at the following locations to provide final corrections:

Card No.	Function(s)
CBBH6	Map maximum range reset. Memory real time reset. Maximum range.
CBFJ6	Interlace.
BAHEØ	Azimuth preset to accommodate interlace.

4.4 SYSTEM CHECKS.

4.4.1 System Digital Sensitivity Test Procedure.

4.4.2 Culmination Test Procedure.

5. TROUBLESHOOTING.

In event the initial checks prescribed in 4.1 indicate a malfunction, the following steps are suggested to assist in isolating the fault. (It is assumed that the system is connected for normal operation and power switch is OFF.)

Step 1. Place site in single-mode interrogation if operationally feasible.

Step 2. Disconnect P/J106.

Step 3. Apply power.

Step 4. Operate in $\overline{\text{STAG}}$ mode.

Step 5. Check +5 V and ±15 V power supplies.

Step 6. Refer to figure 5.1 and check trigger from J1 to B4.

Step 7. In event of difficulty, refer to detailed schematics and effect necessary repairs.

Step 8. Refer to figure 5.2 (a and b) and check stagger clock at C6 (logic). The stagger clock should correspond in time with the first pulse of the input mode trigger.

Step 9. Check ripple clock output of down counter at D22.

Step 10. In event that steps 8 and/or 9 reveal a malfunction, the probable cause is either an incorrect preset of the hexadecimal switch module or an incorrect number of pulses in the input mode trigger. Check that the input mode trigger always contains the same number of pulses and that the hexadecimal preset switch is set for a count of one less than the number of pulses in the mode trigger. If these checks do not reveal the difficulty, it is probable that there has been a component failure. Refer to appropriate drawings.

Step 11. Switch to STAG operation.

Step 12. Check input triggers at A4 (figure 5.1) and staggered triggers at B4. Three sets of mode triggers should be observed at B4 (figure 5.1 shows the difference between STAG and STAG trigger circuitry). If staggered triggers are not available at B4, check at pin 13 of J101, J102, and J103. If not available at any of these points, check appropriate A/S cards, delay line and associated wiring. If triggers are normal at this point, check the SELECT signals at G4, H8, and G7. (For this check, it is advisable to adjust the sweep speed of the scope so that five trigger periods can be observed, but make sure that the sweep is not counting down during retrace.) Observe the signals at G4, H8, and G7. The G4 signal should appear twice, the H8 signal twice, and the G7 signal once during the five-PRT sweep. If these signals are not correct, no definite sequential troubleshooting technique can be prescribed. The system is now in a loop with input (stagger clock) depending on output (staggered P3) and vice-versa. Resolving the problem depends on the knowledge and experience of the individual performing the task.

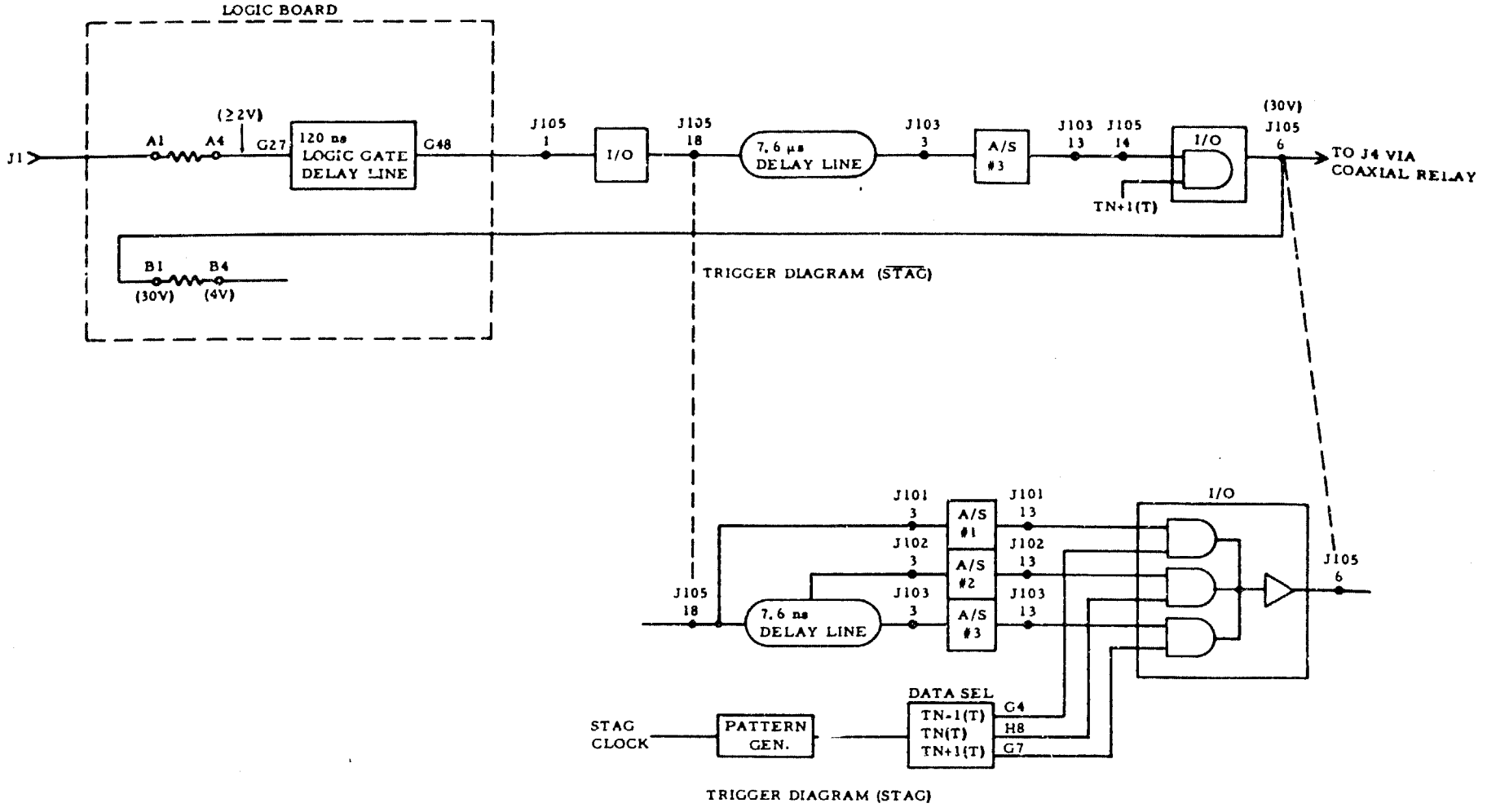
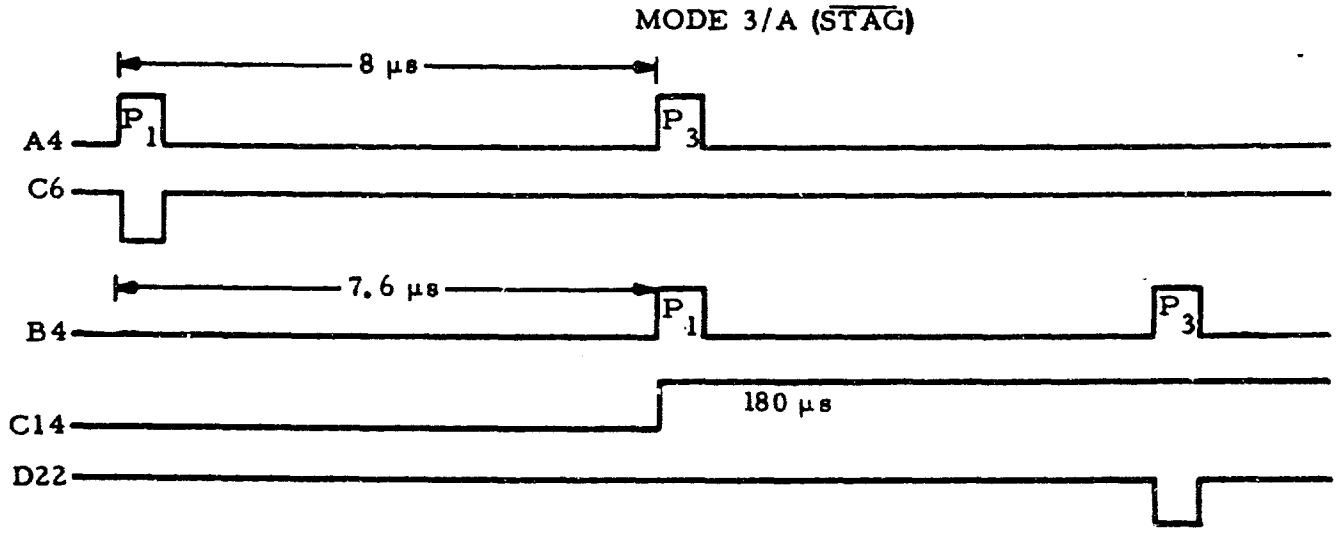
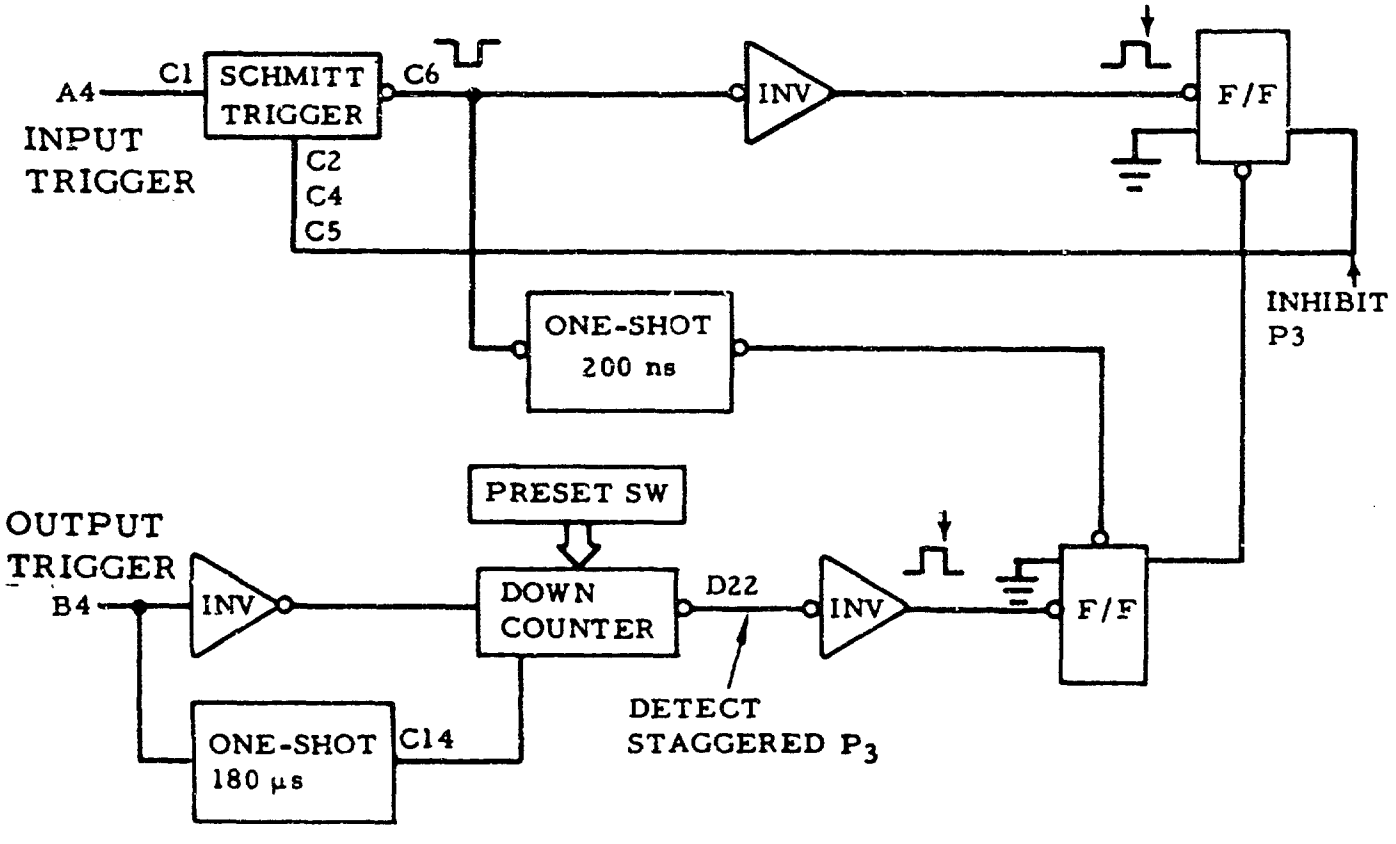


FIGURE 5.1. TRIGGER DIAGRAM



a. TIMING DIAGRAM



b. LOGIC DIAGRAM

FIGURE 5.2. STAGGER/DESTAGGER TROUBLESHOOTING DIAGRAM

6. STAGGER/DESTAGGER SCHEMATICS.

6.1 XD-2707 BLOCK DIAGRAM.

6.2 XD-2706 CONTROL LOGIC.

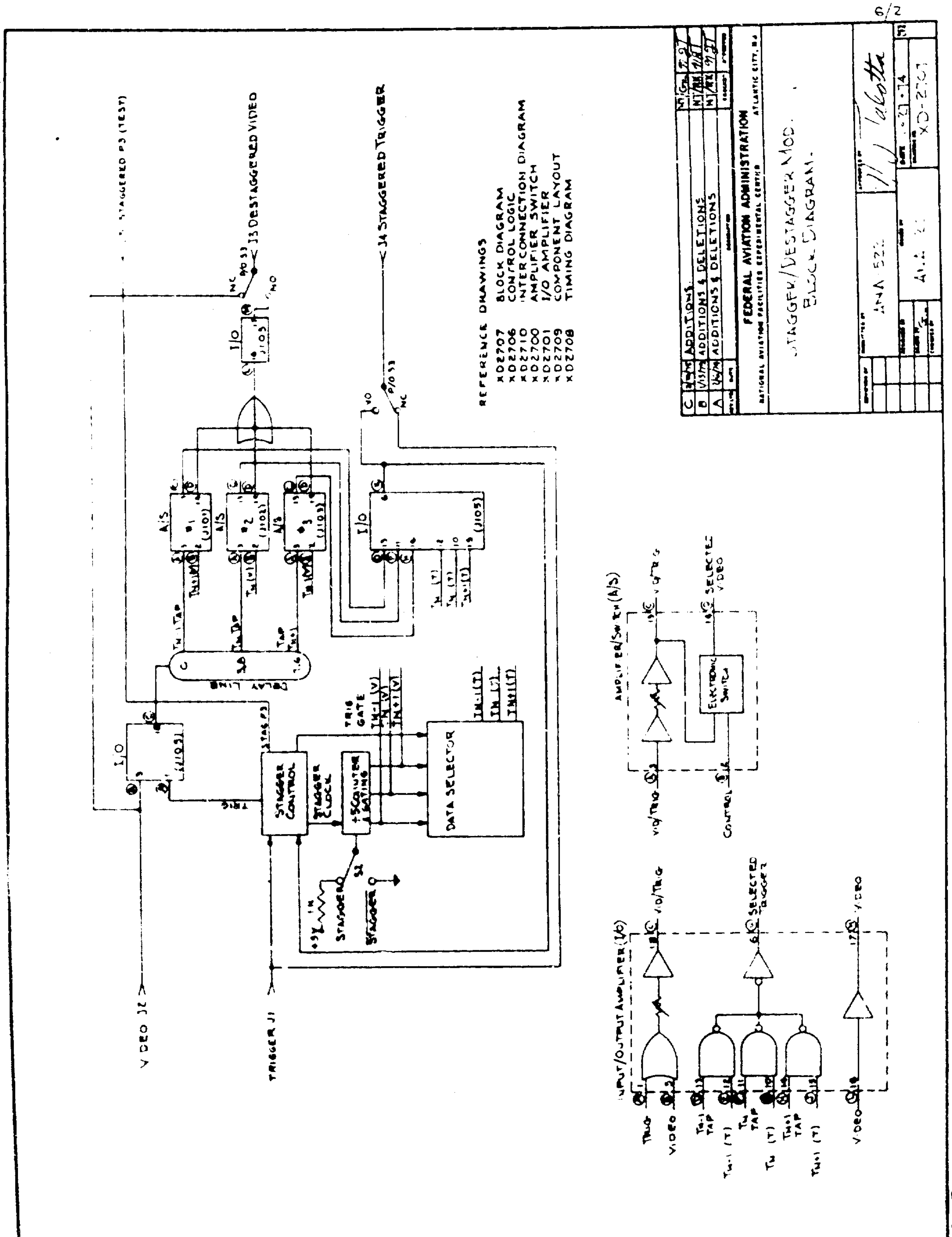
6.3 XD-2710 INTERCONNECTION DIAGRAM.

6.4 XD-2700 AMPLIFIER SWITCH.

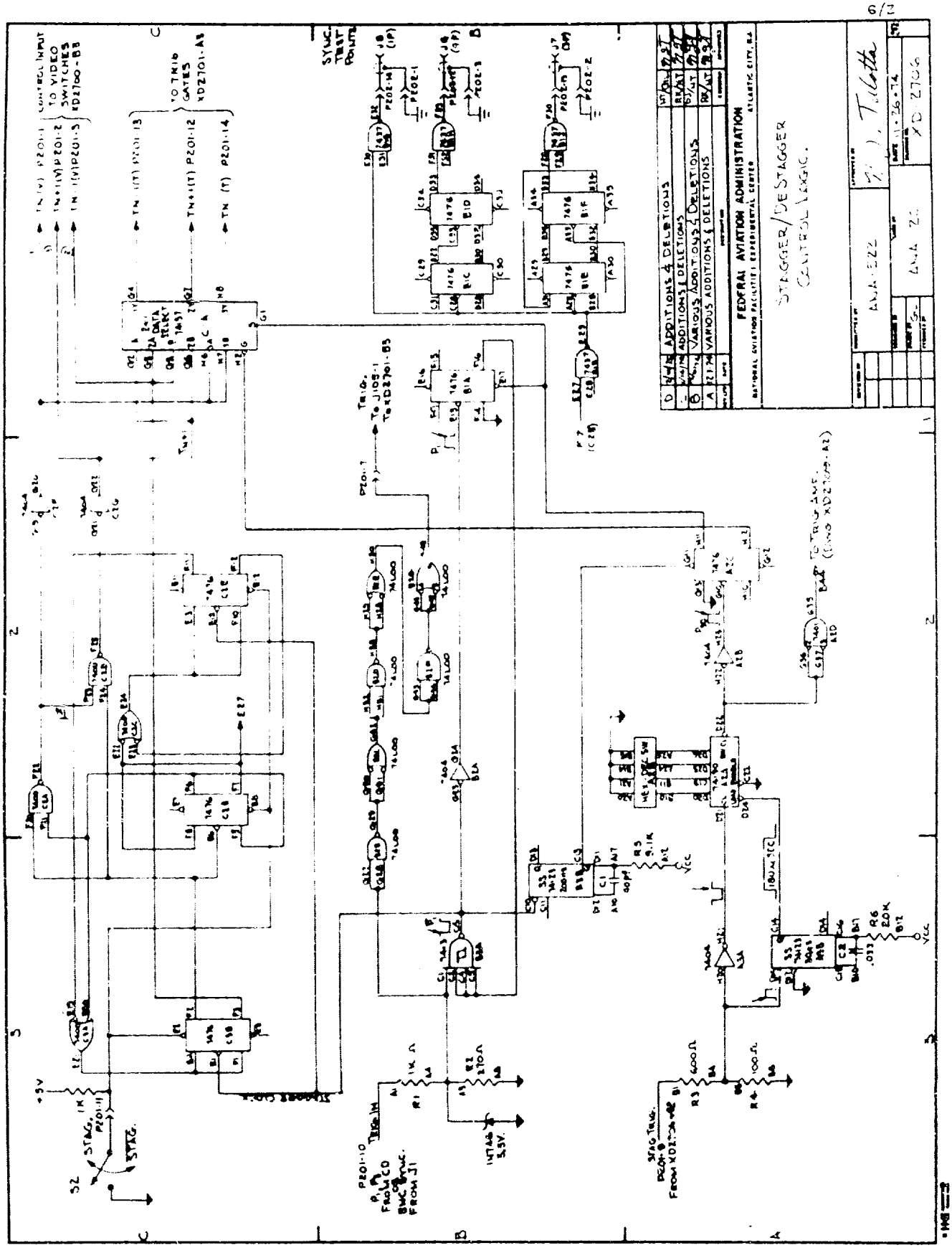
6.5 XD-2701 I/O AMPLIFIER.

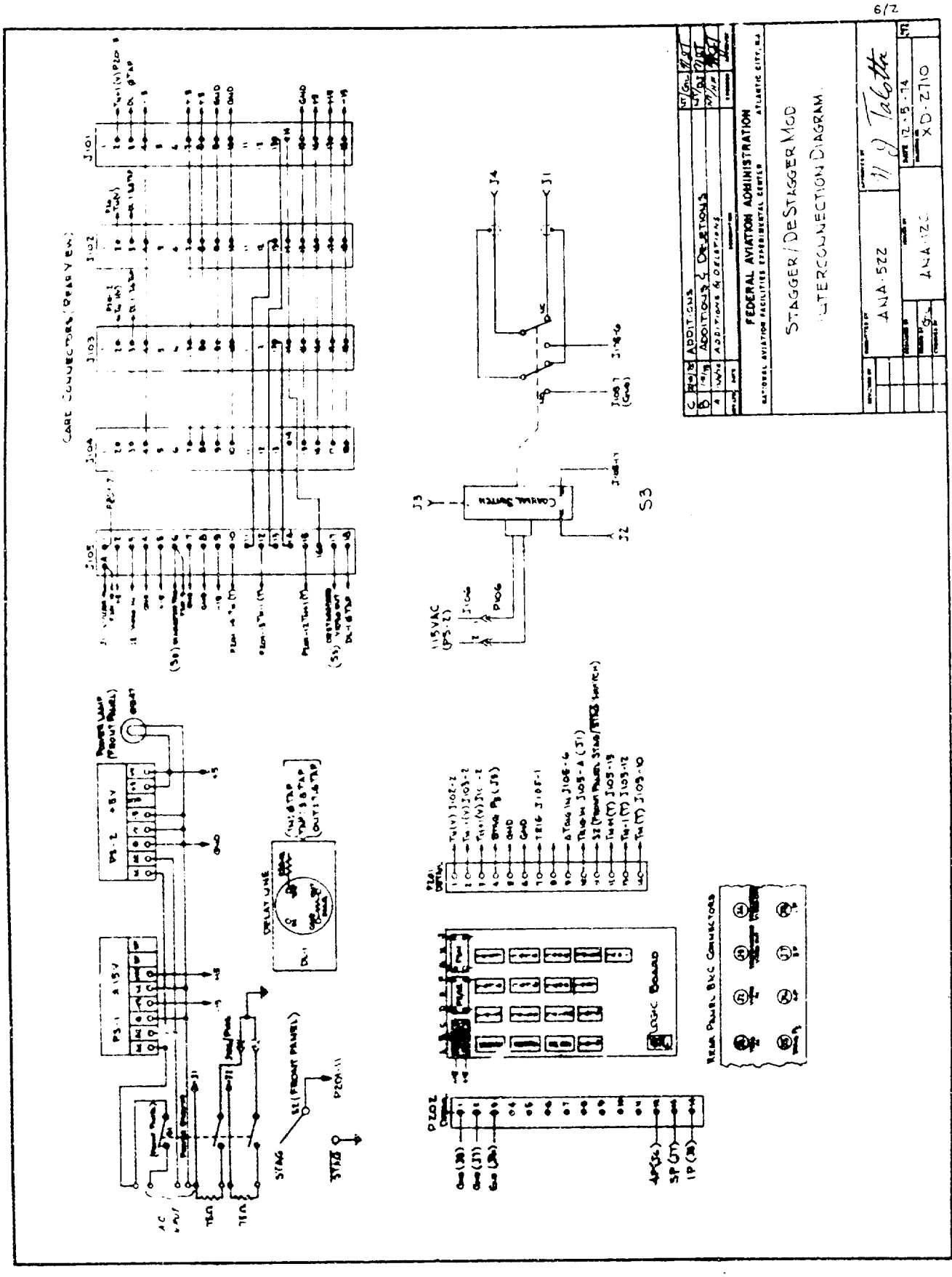
6.6 XD-2709 COMPONENT LAYOUT.

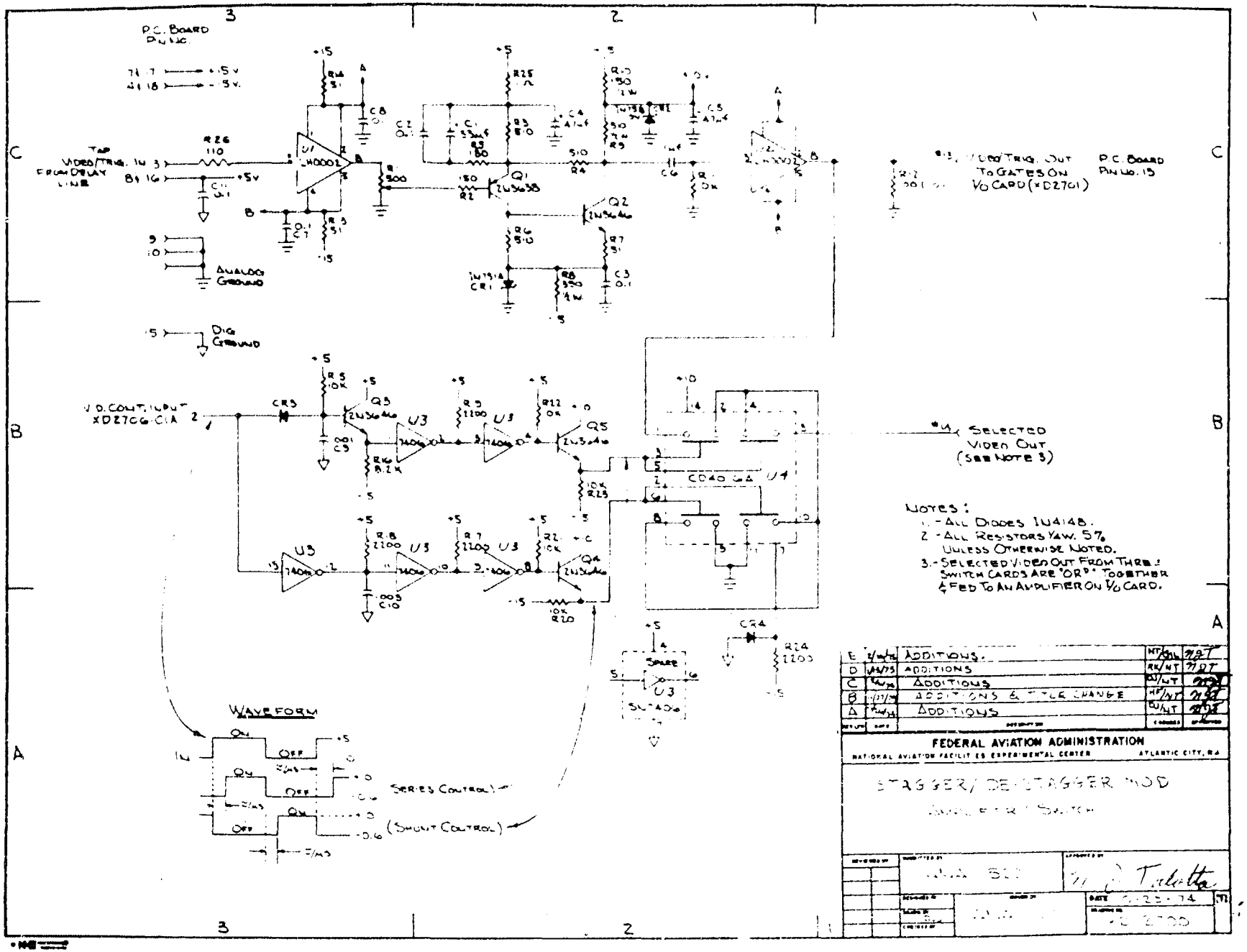
6.7 XD-2708 TIMING DIAGRAM.

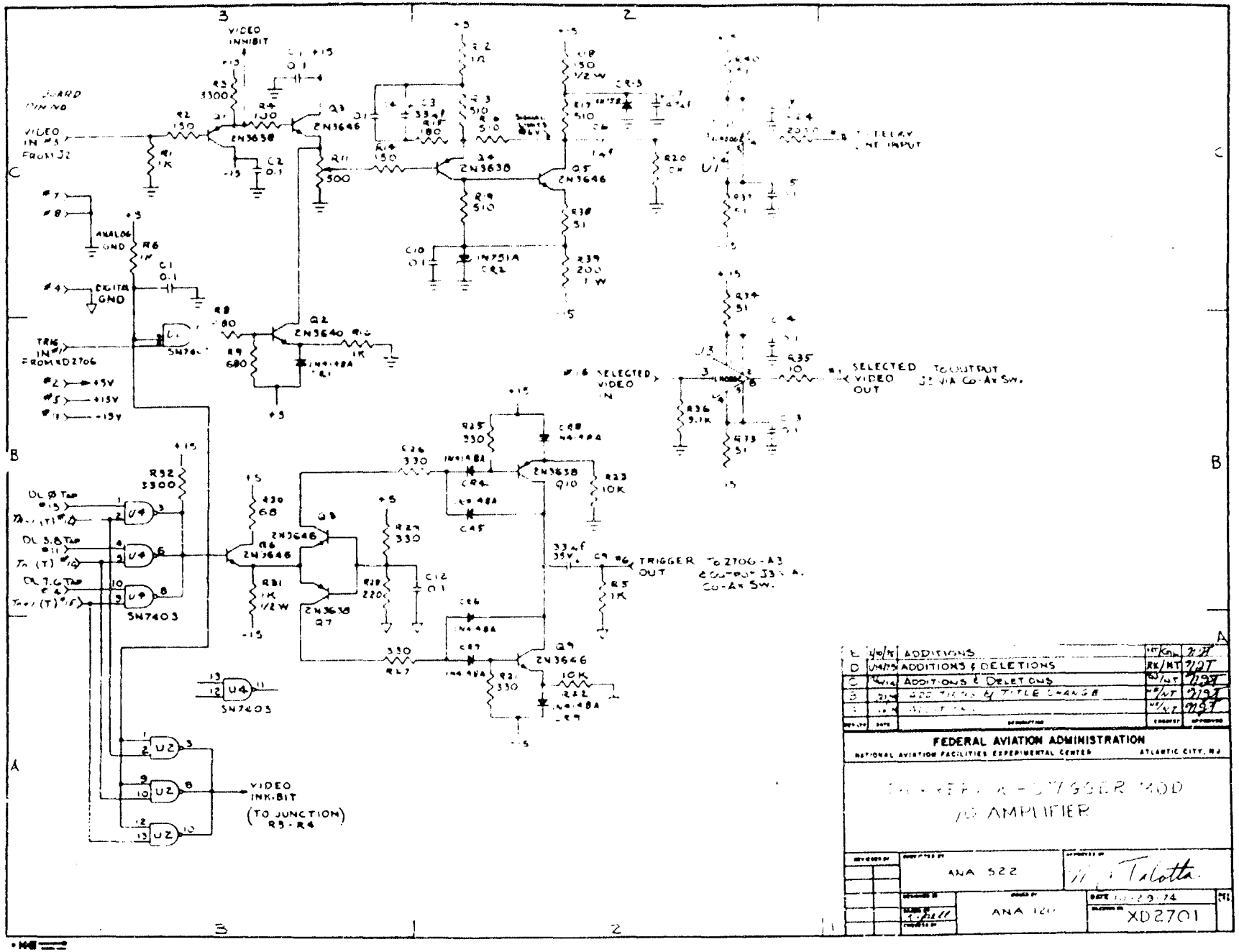


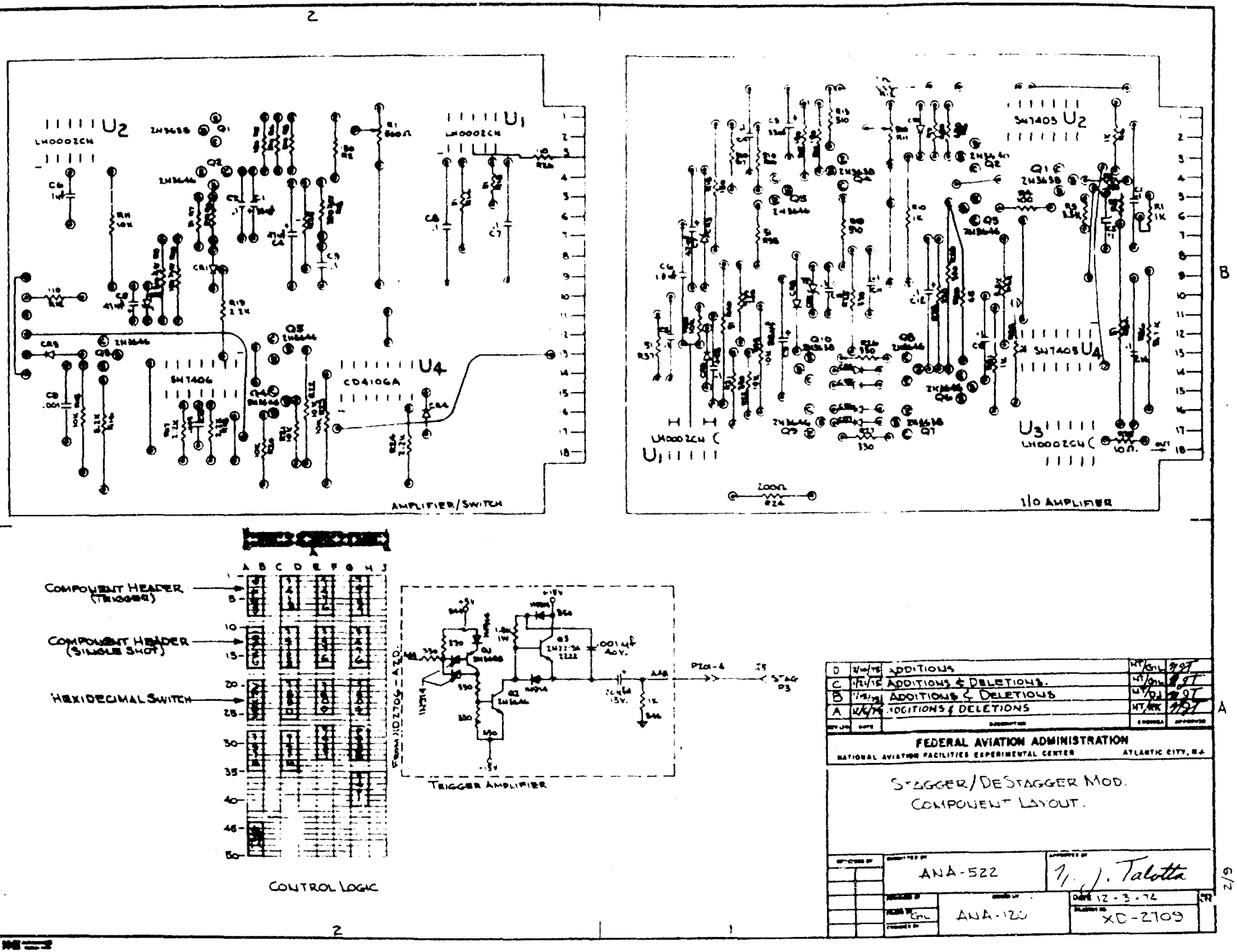
REFERENCE DRAWINGS
XD2707 BLOCK DIAGRAM
XD2706 CONTROL LOGIC
XD2710 INTERCONNECTION DIAGRAM
XD2700 AMPLIFIER SWITCH
XD2701 I/O AMPLIFIER
XD2709 COMPONENT LAYOUT
XD2708 TIMING DIAGRAM
FEDERAL AVIATION ADMINISTRATION
STAGGER/DESTAGGER MOD.
BLOCK DIAGRAM
ANA 522
XD-2707
VIDEO J2
TRIGGER J1
J3 DESTAGGERED VIDEO
J4 STAGGERED TRIGGER
STAGGER CONTROL
DATA SELECTOR
DELAY LINE
STAGGER
ADDITIONS
ADDITIONS & DELETIONS

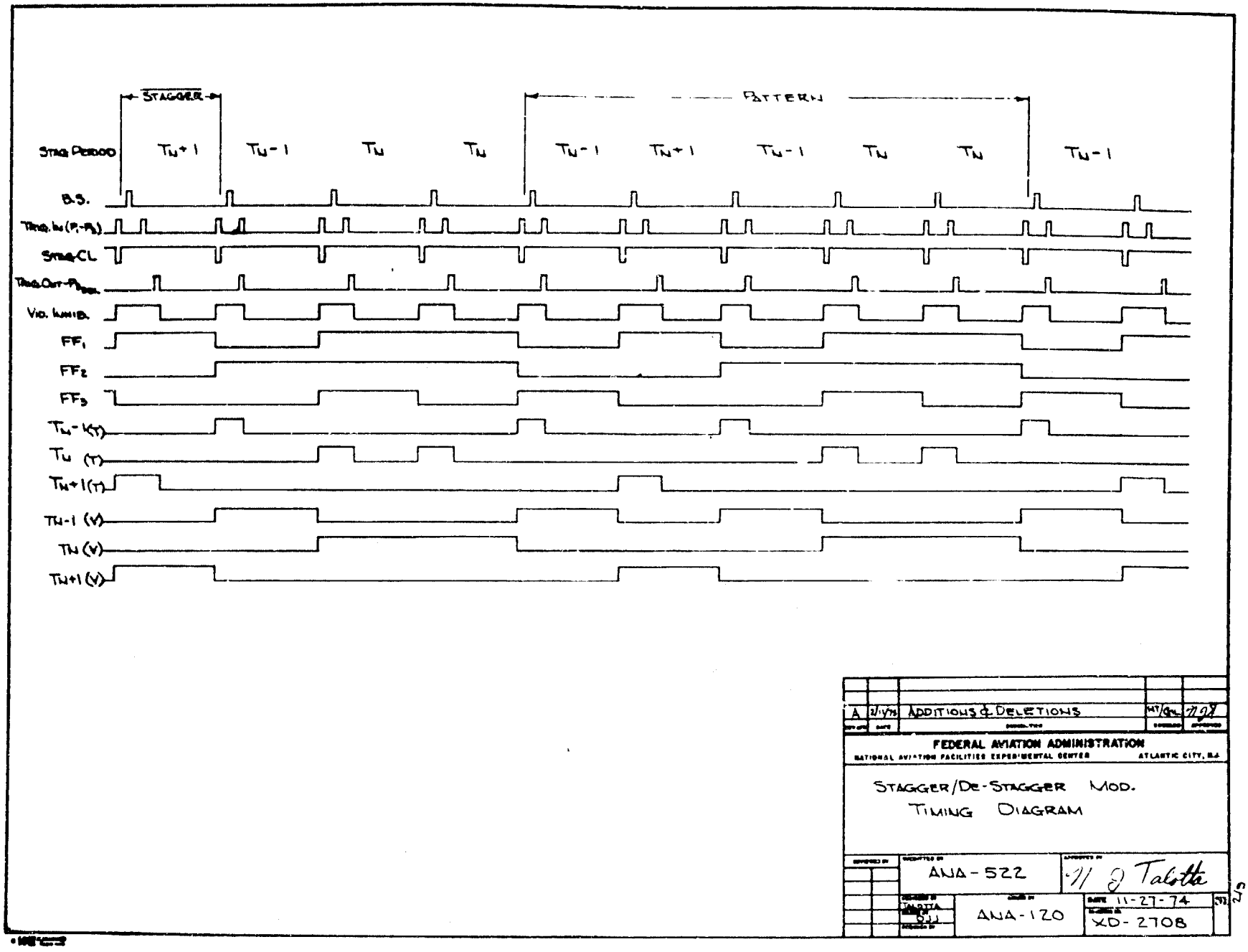

FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, N.J.
STAGGER/DESTAGGER
CONTROL LOGIC
XD 2706
SYNC TEST POINTS
TO TN10 GATES XD2701-A3
TO VIDEO SWITCHES XD2700-B3
STAG.
DESTAG.
+5V
VCC


FEDERAL AVIATION ADMINISTRATION
STAGGER / DESTAGGER MOD
INTERCONNECTION DIAGRAM
ANA-522
ANA-120
XD-2710
ADDITIONS & DELETIONS
CARD CONNECTORS (REAR VIEW)
J101
J102
J103
J104
J105
J4
J1
J3
J2
S3
115VAC
LOGIC BOARD
REAR PANEL BNC CONNECTORS


P.C. BOARD PIN NO.
TAP VIDEO/TRIG. IN 3 FROM DELAY LINE
ANALOG GROUND
DIG GROUND
V.D. CONT. INPUT XDZ7CG-C1A
SELECTED VIDEO OUT (SEE NOTE 3)
VIDEO TRIG. OUT TO GATES ON V/D CARD (XDZ701)
P.C. BOARD PIN NO. 15
CD4016A
WAVE FORM
SERIES CONTROL
SHUNT CONTROL
NOTES:
1. - ALL DIODES 1N4148.
2. - ALL RESISTORS ¼W. 5% UNLESS OTHERWISE NOTED.
3. - SELECTED VIDEO OUT FROM THREE SWITCH CARDS ARE "OR" TOGETHER & FED TO AN AMPLIFIER ON V/D CARD.
E ADDITIONS
D ADDITIONS
C ADDITIONS
B ADDITIONS & TITLE CHANGE
A ADDITIONS
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.
STAGGER/DE-STAGGER MOD
SWITCHER/SELECTOR
DATE 4-25-74


VIDEO INHIBIT
BOARD SYM NO
VIDEO IN #3 FROM J2
ANALOG GND
DIGITAL GND
TRIG IN #7 FROM XD2706
#2 +5V
#5 +15V
#1 -15V
SN7403
SN7405
VIDEO INHIBIT (TO JUNCTION R3 - R4
#6 SELECTED VIDEO IN
SELECTED VIDEO OUT TO OUTPUT J2 VIA CO-AX SW.
TRIGGER OUT TO 2706 - A3 & OUTPUT J3 VIA CO-AX SW.
TO DELAY LINE INPUT
ADDITIONS
ADDITIONS & DELETIONS
ADDITIONS & DELETIONS
ADDITIONS & TITLE CHANGE
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, N.J.
VIDEO & TRIGGER MOD TO AMPLIFIER
ANA 522
ANA 121
XD2701


U2
LH0002CH
U1
LH0002CH
U4
CD4016A
SN7406
AMPLIFIER/SWITCH
SN7405 U2
U4
SN7405
U3
LH0002CH
U1
LH0002CH
I/O AMPLIFIER
COMPONENT HEADER (TRIGGER)
COMPONENT HEADER (SINGLE SHOT)
HEXIDECIMAL SWITCH
CONTROL LOGIC
TRIGGER AMPLIFIER
D 2/14/72 ADDITIONS
C 12/12/72 ADDITIONS & DELETIONS.
B 7/31/72 ADDITIONS & DELETIONS
A 4/4/72 ADDITIONS & DELETIONS
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, N.J.
STAGGER/DESTAGGER MOD.
COMPONENT LAYOUT.
ANA-522
ANA-120
12-3-72
XD-2709


STAGGER
PATTERN
STAG PERIOD
TN+1
TN-1
TN
TN
TN-1
TN+1
TN-1
TN
TN
TN-1
B.S.
TRIG. IN (P1-P3)
STAG CL
TRIG. OUT-P1 DEL.
VID. LUM I.D.
FF1
FF2
FF3
TN-1 (T)
TN (T)
TN+1 (T)
TN-1 (V)
TN (V)
TN+1 (V)
A
ADDITIONS & DELETIONS
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, N.J.
STAGGER/DE-STAGGER MOD.
TIMING DIAGRAM
ANA-522
ANA-120
11-27-74
XD-2708

APPENDIX B

DIGITAL STAGGER EQUIPMENT MODIFICATION

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

TABLE

1. INTRODUCTION.

The function of the beacon stagger/destagger modification is to prevent second-time-around targets from appearing as valid targets at some pseudo range in the reply processing system.

Consider a beacon system with a pulse recurrence time (PRT) of 2000 microseconds (μs) and a target located at a range of 2500 μs. During the first interrogation period in which the target is illuminated by the antenna beam no reply will be received. Five hundred microseconds after the second interrogation, reply video from the first interrogation will be received. This condition of reply video appearing 500 μs into the interrogation period following the interrogation period which actually generated the reply will continue until the target is no longer illuminated by the antenna beam. Reply processing equipment will indicate a target at a range of 500 μs when, in fact, no such target exists.

The beacon stagger/destagger modification eliminates such false targets by introducing a trigger/video delay of 7.2 μs in three different combinations as shown in table 1. In the combination designated TN+1, the trigger is delayed 7.2 μs and the video is not delayed. In the combination designated TN, both the trigger and video are delayed 3.6 μs. In the combination designated TN-1, the trigger is not delayed and the video is delayed 7.2 μs.

TABLE 1. BEACON STAGGER/DESTAGGER MODE TIMING

Mode	Delay (μs)	
	Trigger	Video
TN+1	7.2	0
TN	3.6	3.6
TN-1	0	7.2

A single delay line is used to provide the delays for the staggering as well as the destaggering process. The characteristics of the delay line that are important include a temperature coefficient which is consistent with the delay accuracy requirement of 7.2 ±.025 μs, and a delay-to-rise time ratio that will not significantly degrade TTL video pulses. Rise time, fall time, overshoot, ringing, and sag must be TTL compatible.

The system is implemented by selecting an appropriate mode at the beginning of each interrogation period. Mode selection is in accordance with a predetermined pattern of TN-1, TN+1, TN-1, TN, TN. The pattern is established by a hard-wired logic system and is repetitive as long as the system is operating in the stagger mode. In nonstagger the system operates in the TN+1 mode only.

Assume a system with a PRT of 2,000 μs operating in the nonstagger mode with a target at a range of 1,000 μs with respect to beacon sync. Assume further that the system is switched to stagger operation and the stagger mode becomes TN-1. This mode implies the interrogation triggers will occur at range zero minus 7.2 μs, and the reply video must be delayed by 7.2 μs in order

for the target to appear at a range of 1,000 μs. Similarly, when the pattern switches to the TN mode, the trigger timing with respect to beacon sync is changed by 3.6 μs, and the video reply path must be changed by the same increment of time in the opposite direction. On successive interrogations, first-time targets will maintain a fixed-time relationship with beacon sync, but second-time-around targets will vary in time by 3.6 or 7.2 μs with respect to beacon sync and will be removed from the system by conventional defruiter or common-digitizer (CD) equipment.

2. THEORY OF OPERATION.

2.1 GENERAL. (See drawing XD-2725, sheet 1.)

To implement stagger/destagger, it is necessary to change the timing relationship between a stable source trigger (i.e., beacon sync) and mode triggers from PRT to PRT. When the mode triggers are staggered, it is necessary to maintain the video in the original time relationship with beacon sync. The video must therefore be shifted in time (destaggered) by the same amount as the triggers are staggered, but in the opposite direction in reference to time.

Input to the system consists of the source trigger and receiver beacon video. The output consists of staggered trigger, destaggered video, a staggered sync trigger, and a pattern sync trigger.

The input video is processed via a quantizer and pulse width discriminator prior to destaggering. The quantizer produces a transistor-transistor logic (TTL) video pulse with a width equal to the width of the input pulse at its half-amplitude points. The pulse width discriminator rejects pulses less than 150 nanoseconds (ns) wide and is adjustable to reject pulses up to 300 ns wide. Video from the pulse width discriminator is used as the input to the stagger/destagger delay line which is a center-tapped lumped constant line with a total delay of 7.2 μs.

The input triggers are also fed to the stagger/destagger delay line after they are interfaced to TTL and delayed for approximately 130 ns. Trigger stagger and video destagger is accomplished by selecting a specific tap of the stagger/destagger delay line for triggers and a specific tap for video during each PRT. The tap selection is accomplished by conventional logic gating controlled by a pattern generator.

2.2 NAFEC QUANTIZER (NAQ) (See figure 2-1 and drawing XD-2725, sheet 2.)

The National Aviation Facilities Experimental Center (NAFEC) quantizer (NAQ) suppresses the noise output of a beacon receiver and converts the receiver video to a TTL pulse whose width is equal to the half-amplitude width of the original signal.

The key components of the system are a delay line and four differential comparators with a TTL output. The differential comparators appear on the schematics as triangles with two input lines and one output line. When the

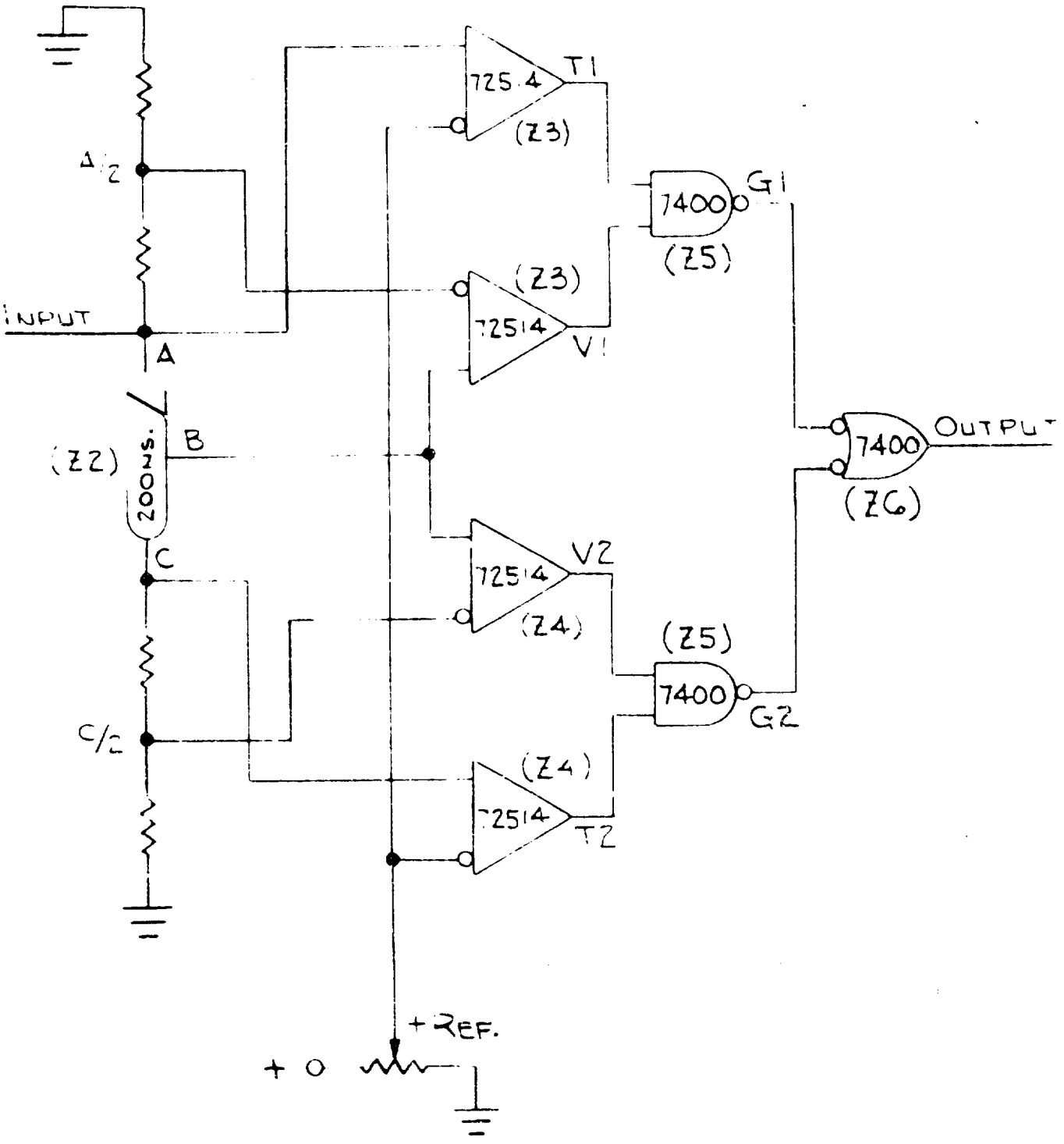


FIGURE 2-1. NAFEC QUANTIZER

inverting (circled) input voltage is positive with respect to the noninverting (uncircled) input voltage, the output line is low (approximately zero volts). When the noninverting input voltage is positive with respect to the inverting input, the output line goes high (approximately +4 volts).

The +REF voltage is set to a point just above the average peak noise level of signal at the input (A) to the delay line. The output line of each threshold differential comparator will be low except when a video pulse is received or random noise spikes exceed the threshold setting.

The input video is fed simultaneously to the delay line and to a resistive divider network, the center of which provides a half-amplitude signal. The terminating resistance of the delay line is likewise divided into two equal resistors to provide a half-amplitude signal at the output. The half-amplitude input and output signals are compared, in two separate comparators, with the full-amplitude signal from the center tap of the delay line.

When the input signal consists only of noise, the outputs of the two threshold comparators (T1 and T2) will be low. Therefore, the outputs of gates (G1 and G2) will be high. During this period the outputs of the video comparators (V1 and V2) will contain noise since the noise at B will exceed the noise at A/2 and C/2. When a video pulse is received, T1 goes high enabling one input to G1. V1 goes low until the leading edge of the pulse reaches the delay line center tap (B). V1 then goes high for the duration of the pulse at B. With both inputs to gate No. 1 high, G1 output goes low, and the quantizer output goes high through the output NOR gate. The V2 output goes high at the same time that V1 goes high, enabling one input to gate No. 2. T2 goes high 200 ns after T1 and enables the second input to gate No. 2. The G2 output also produces a quantizer output through the output NOR gate.

When the trailing edge of the input pulse passes point A, T1 goes low and prevents any output of V1 from reaching the output NOR gate. When the trailing edge of the pulse passes point B, the output of V2 goes low, thus terminating the output of G2 and the output NOR gate.

2.3 PULSE WIDTH DISCRIMINATOR. (See figure 2-2 and drawing XD-2725, sheet 2.)

The pulse width discriminator rejects pulses which are less than a predetermined width. The rejection point is established by setting the potentiometer associated with the single-shot multivibrator SS-1. SS-2 is set to the same pulse width as SS-1 in order to restore valid pulses to their original width.

Incoming quantized video passes through the two type 7408 gates to one input of a type 7400 NAND gate. The leading edge of the incoming video also triggers SS-1 to its unstable state, causing the $\bar{Q}$ output to go low. The $\bar{Q}$ output of SS-1 is connected to the second input of the type 7400 NAND gate and thus inhibits the gate for the duration of the SS-1 unstable state condition. If the incoming video pulse width exceeds the width of the SS-1 unstable state output, the difference width will be passed through the 7400 NAND gate.

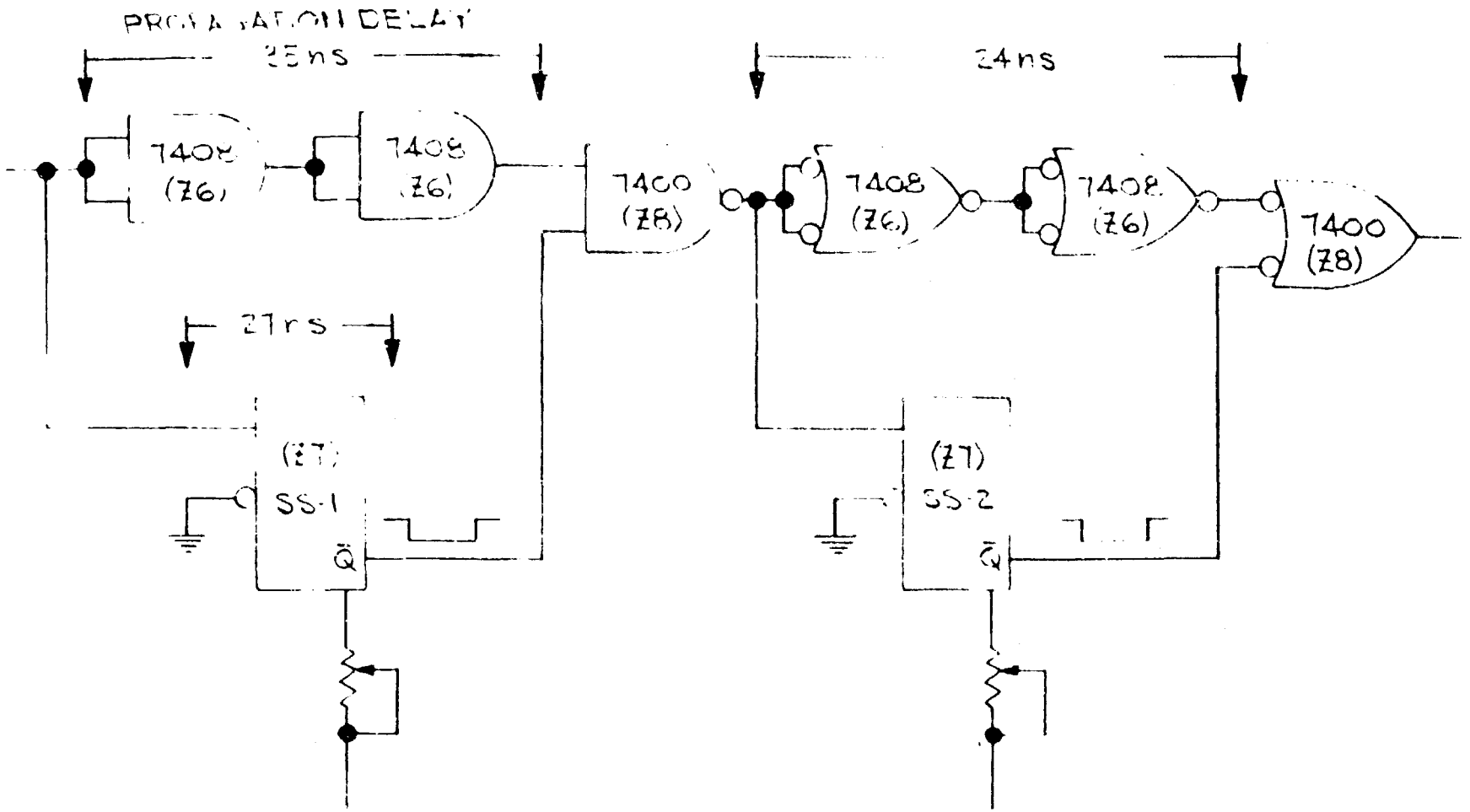


FIGURE 2-2. PULSE WIDTH DISCRIMINATOR

The difference width output of the 7400 NAND gate (a negative pulse) is passed through two type 7408 gates to one input of a type 7400 IC chip used in a NOR configuration. This input appears as a positive pulse at the output of the NOR gate.

The trailing edge of the negative pulse from the type 7400 NAND gate triggers SS-2 into its unstable state. The $\overline{Q}$ output of SS-2, which is low during the unstable state, is connected to the second input of the 7400 NOR gate and extends the output of the gate.

With SS-1 and SS-2 adjusted for equal pulse width, input video with a duration less than SS-1 will be inhibited, and video with a duration greater than SS-1 will be passed through the discriminator and appear at the output at its original width. Note, however, that the output pulse will be delayed by an amount at least equal to the duration of SS-1.

2.4 PATTERN GENERATOR. (See figure 2-3 and drawing XD-2725, sheet 3.)

The pattern generator consists of four D-type flip-flops and associated gates. It operates as a ring counter in that only one of the three flip-flops (designated TN-1, TN+1, TN) is "set" during a trigger period. The fourth flip-flop is a control device to provide the levels necessary for proper sequential operation of the other three flip-flops.

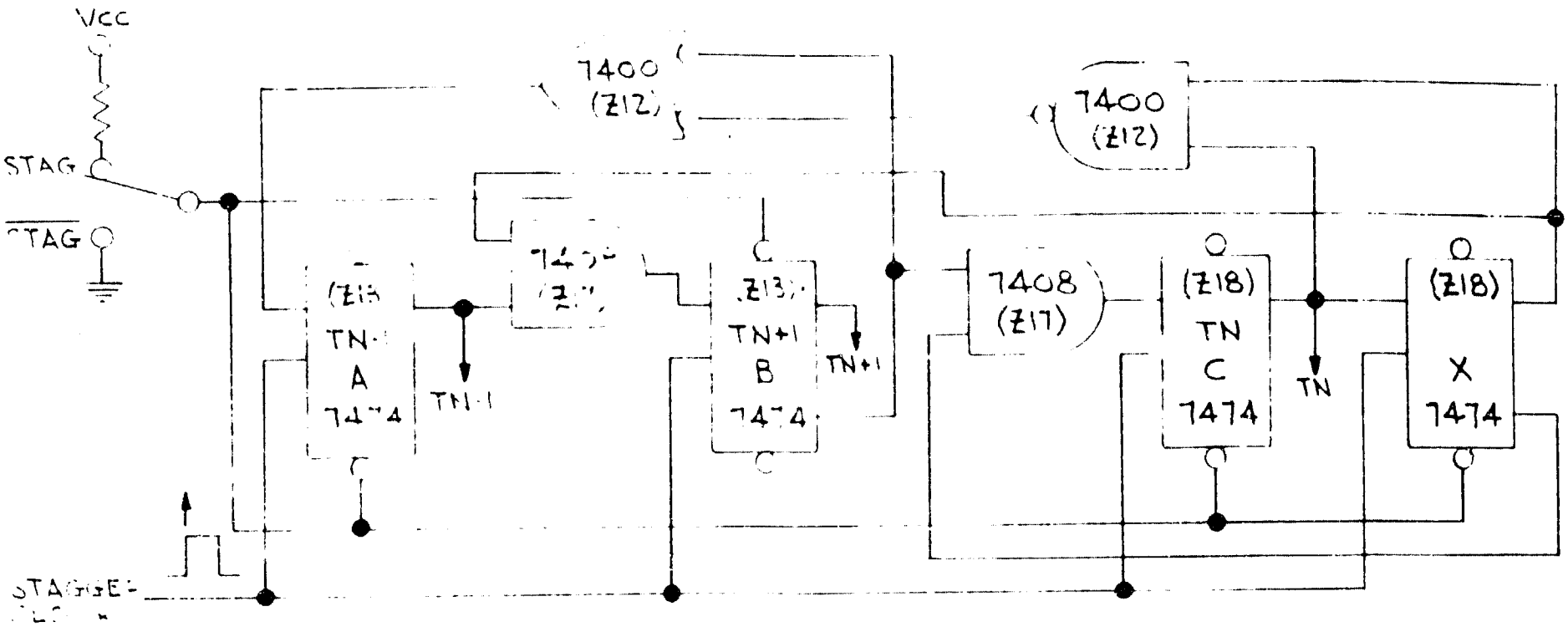
With the front panel control switch in the nonstagger ($\overline{STAG}$) position, the TN+1 FF will be "set," and all others will be "reset." The stagger clock will have no effect on the operation. When the control switch is in the stagger (STAG) position, the stagger clock will step the counter to produce the desired sequential pattern.

2.5 TRIGGER INPUT CONTROL. (See figure 2-4 and drawing XD-2725, sheet 3.)

The trigger control circuitry shapes and delays the input trigger(s), gates the video and triggers into the lumped constant stagger delay line, and generates a stagger clock to operate the pattern generator.

2.5.1 Trigger Interface. The trigger input interface circuit is a resistive voltage divider and a 3.3 volt (V) zener diode. The component values allow the system to operate with positive triggers from 8 to 70 V. Either single pulses (i.e., beacon sync) or mode pulse pairs may be used as input triggers by making the appropriate jumper connection from S (single) or D (double) to C (common) at the trigger input to FF-3. Double pulse operation is assumed in the following discussion.

2.5.2 Input Timing. From the input divider, the trigger is processed through a Schmitt trigger whose output is a negative TTL pulse. The leading edge of the pulse triggers SS-1, which produces a positive-going pulse of approximately 50-μs duration. The duration of this pulse is not critical, the requirement being that the "preset" input to FF-2 be lifted for a period equal to the greatest mode pulse spacing (mode D=25 μs), plus the longest stagger delay (7.2 μs).



SEQUENCE

	A	B	C	X	
TN-1	1	0	0	1	A = B + CX
TN+1	0	1	0	0	B = AX
TN-1	1	0	0	0	C = $\overline{B}\,\overline{X}$
TN	0	0	1	C	X = C
TN	0	0	1	1	

FIGURE 2-3. PATTERN GENERATOR

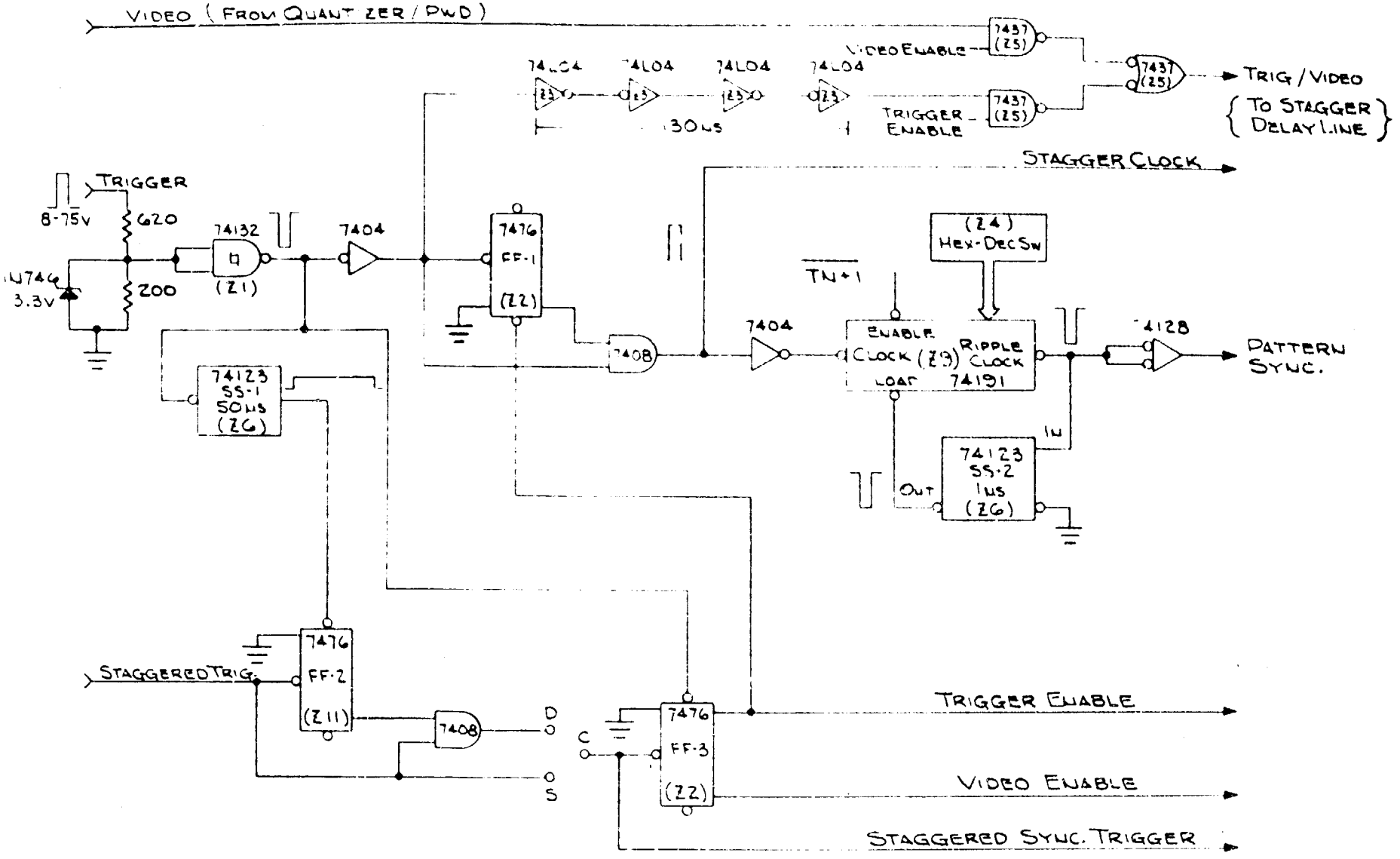


FIGURE 2-4. TRIGGER CONTROL

The negative output pulse from the Schmitt trigger also "sets" FF-3. This removes the "clear" from FF-1 and also produces the TRIGGER ENABLE signal.

The negative Schmitt output is inverted through a 7404 and follows three paths. In the lower path, the pulse is ANDed in a 7408 with the $\bar{Q}$ output of FF-1 and becomes the STAGGER CLOCK to the pattern generator. In the upper path, the pulse is fed through four type 74L04 hex inverters, the sole purpose of which is to delay the pulse by approximately 130 ns so that the pattern generator may assume a new state prior to the trigger entering the stagger delay line. In the center path, the trailing edge of the pulse triggers FF-1 to the "set" state. This prevents the second pulse of the mode trigger pulse pair from generating a second stagger clock during the same interrogation period.

From the 74L04 hex inverters, the trigger pulses are ANDed with the TRIGGER ENABLE signal, NORed with the video, and routed to the stagger delay line. Depending on the pattern signal for the particular interrogation period under consideration, the triggers will be gated out of one of three taps of the stagger delay line (i.e., zero, 3.6 or 7.2 μs). In addition to being amplified and distributed as output triggers, the triggers are fed back to the trigger control circuitry at the point labeled STAGGERED TRIGGER.

At the time the first staggered trigger arrives, FF-2 is in the "set" state but the "preset" input has been lifted by the action of SS-1, and therefore FF-2 is free to toggle. Since it toggles on the trailing edge of the pulse, the first pulse cannot pass through the 7408 gate. The trailing edge of the pulse causes FF-2 to go to the "reset" state, therefore, the second pulse of the staggered trigger output passes through the 7408 gate and becomes the staggered sync trigger. The trailing edge of the staggered sync trigger "resets" FF-3, thus terminating TRIGGER ENABLE and generating VIDEO ENABLE.

The staggered sync trigger is fed via a trigger amplifier to a rear-panel BNC connector for use with external equipment. When SS-1 returns to its stable state, FF-2 is "preset" and is held in this state until receipt of the next input trigger pulse. This prevents FF-2 from remaining "out-of-step" in the event of an extraneous or missing pulse during an interrogation period.

2.5.3 Pattern Sync Generator. Associated with the trigger control circuitry is the pattern sync generator consisting of an inverter, down-counter, hexadecimal switch, single shot and an output line driver. The function of the pattern sync generator is to produce a sync pulse once per pattern (five interrogation periods) or once per n patterns. The latter condition is to facilitate observation of signals during various interlace ratios. With the hexadecimal switch set at "zero," a pattern sync pulse will be generated once per five interrogation periods at the beginning of the TN+1 period. If the system is operating in two modes with a one-to-one interlace ratio, the hexadecimal switch can be set at "one," and a pattern sync pulse will be generated once per 10 interrogation periods. For other mode interlace ratios, the hexadecimal switch can be set accordingly. The sync pulse will always be

generated at a pattern count one greater than the switch setting. The pattern sync pulses are routed to a front panel BNC connector for each channel.

2.6 VIDEO INPUT CONTROL. (See figure 2-4 and drawing XD-2725, sheet 3.)

Video from the quantizer/pulse width discriminator circuitry is routed through the trigger control and NORed with the triggers to the stagger delay line. The video is gated into the NOR gate by the VIDEO ENABLE signal. Since VIDEO ENABLE and TRIGGER ENABLE are complementary outputs of FF-3, only video or only triggers can be gated into the delay line at any one time.

2.7 TRIGGER/VIDEO OUTPUT CONTROL. (See figure 2-5 and drawing XD-2725, sheet 3.)

Trigger and video output control is basically just a matter of gating stagger delay line taps with appropriate pattern signals. A given pattern signal is "high" for one interrogation period. During the TN+1 pattern segment, triggers are gated from the 7.2 μs tap and video from the zero tap. During TN-1, triggers are gated from the zero tap, and video from the 7.2 μs tap. During TN, both triggers and video are gated from the 3.6 μs tap.

The outputs of the three trigger NAND gates are combined in a NOR gate whose output is "ANDED" with the TRIGGER ENABLE signal. This prevents subsequent video in the delay line from being processed as triggers. The output of the trigger AND gate is fed back to the trigger control circuitry and to a trigger amplifier for distribution to external equipment.

The video is similarly processed and fed to 75-ohm line drivers for external distribution at TTL levels.

2.8 TRIGGER AMPLIFIER. (See figure 2-6 and drawing XD-2725, sheet 2.)

The function of the trigger amplifier is to provide amplification and drive capability for triggers to external equipment.

In the quiescent state, Q1 and Q2 are "ON," and Q3 is "OFF." Minus 12 V appears at the negative side of the output capacitor C15. When an input trigger is received, Q1 is cut off causing Q2 to cut off, and Q3 starts conducting. As Q3 starts to conduct, the voltage at C15 starts to rise. This rise is coupled through C14 to the top of R24 in a bootstrap action which accelerates and insures the complete turn-on of Q3. The change in voltage from -12 to +12 V on the negative side of C15 appears as a zero to +24 V change on the plus side of C15.

2.9 POWER SUPPLIES. Direct current (d.c.) voltages required to power the system are ±5 V and ±12 V. Two dual power supplies are installed for each channel.

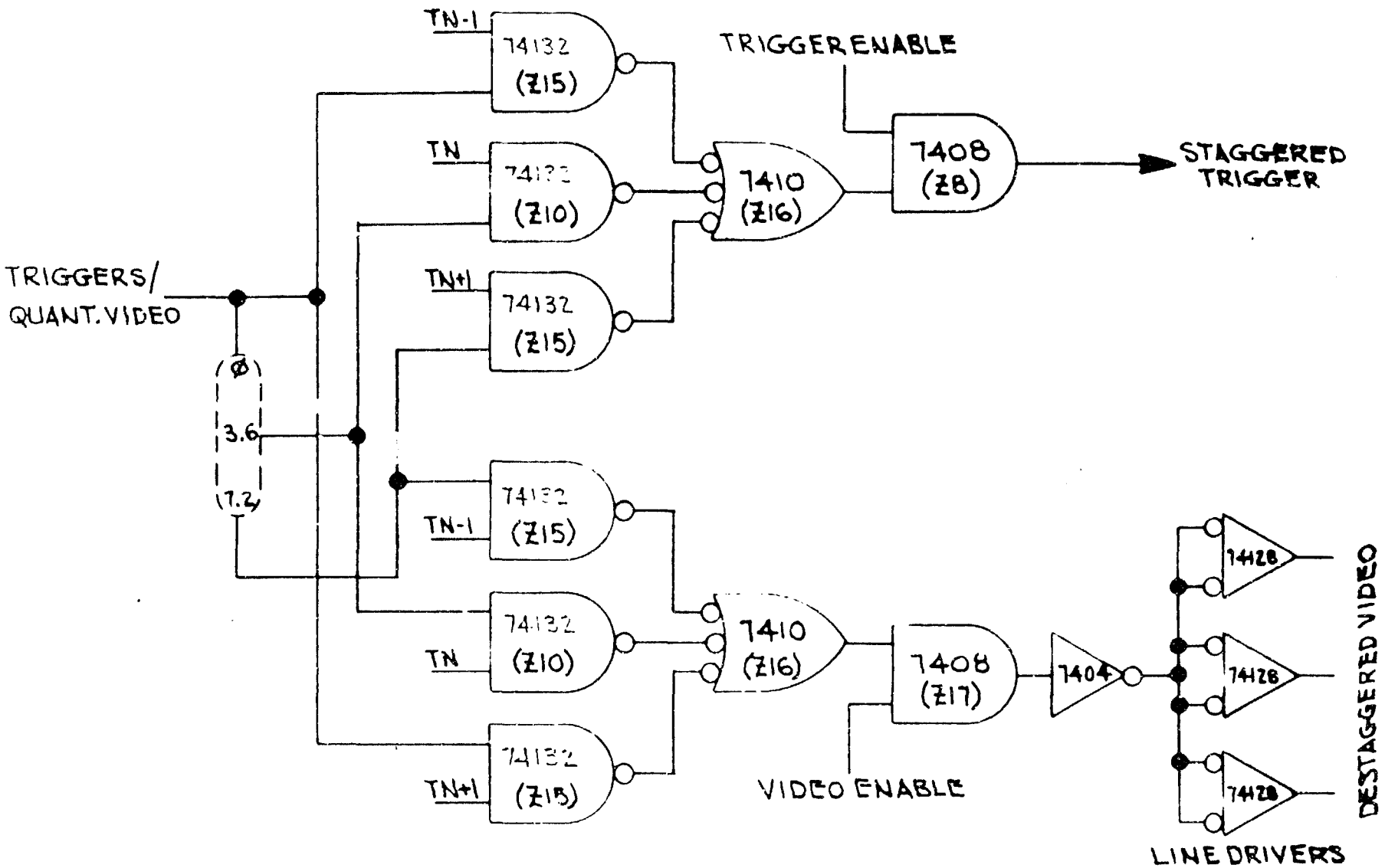


FIGURE 2-5. TRIGGER/VIDEO OUTPUT CONTROL

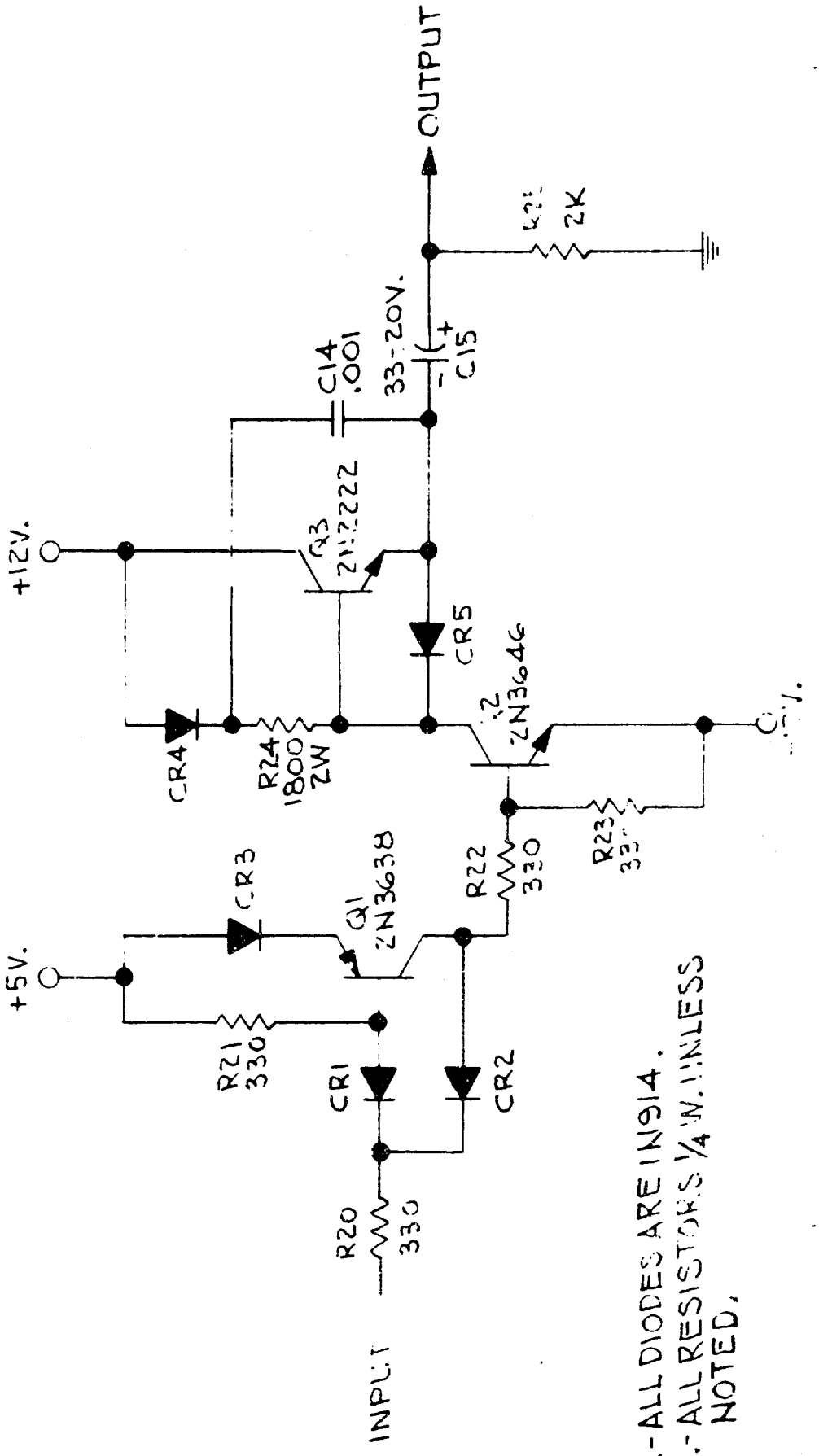


FIGURE 2-6. TRIGGER AMPLIFIER

3. INSTALLATION.

The STAGGER/DESTAGGER modification chassis is fabricated in a dual channel configuration in a standard size chassis equipped with rack slides for mounting in a 19-inch rack. Input power requirements are 115-V alternating current (a.c.) 47 to 420 hertz (Hz). Maximum power dissipation is 102 watts.

Signal connections consist of trigger in (J1), receiver video in (J3), staggered trigger out (J2), and destaggered video out (J4). The input trigger and video signals are internally paralleled to both channels. The output trigger and video signals are switched via front panel control S5. The control S5 is a manually operated coaxial switch. The switch handle is positioned to the left for channel 1 and to the right for channel 2.

Channel 1 and channel 2 staggered sync triggers are provided at rear-panel jacks J5 and J6, respectively. The sync triggers correspond to staggered beacon sync or staggered P3, depending on the input trigger source (beacon sync or mode pulse pair).

Pattern sync and video output for each channel are provided on appropriately labeled front-panel BNC connectors for convenience during test and monitoring.

The period between pattern sync pulses is controlled by the setting of the HEX-DEC switch located on the logic card. With the switch set at zero, the pattern sync pulse will occur once per 5 PRT's.

Power to each channel is controlled by separate double-pole single-throw toggle switches. Both sides of the powerline to the power supplies are opened when the switch is "OFF."

4. ADJUSTMENTS.

4.1 STAGGER/DESTAGGER ADJUSTMENTS.

Two circuits in the system require adjustment. These are the threshold in the quantizer and the width controls in the pulse width discriminator. All three adjustments are located on the top edge of the quantizer card. The threshold adjustment (R17) is the control closest to the front panel. R19 is the center adjustment and controls the second single-shot in the pulse width discriminator. The setting of the control restores a valid pulse to its original input width.

The third adjustment (R18) controls the first single-shot in the PWD and determines the minimum pulse width which will pass through the PWD. The range of adjustment of each single shot is approximately 150 to 300 ns.

Adjustment of R17 (threshold) depends upon the average peak noise level of the receiver. Threshold is set just above this point. To adjust the threshold insert a test signal into the receiver a few decibels above tangential sensitivity. With the system in nonstagger, observe the output of the desired

stagger/destagger channel on an oscilloscope. If the initial threshold setting is too low (R17 CCW), excessive noise will be observed on either side of the test pulse. If the initial threshold setting is excessively high (R17CW), no output will be observed. Adjust R17 for minimum noise on either side of the test video pulse with no break-up of the pulse itself. Reduce the test signal into the receiver to tangential sensitivity level. Readjust R17 for approximately equal test pulse baseline break-up and noise.

Adjust R18 (pot closest to connector end of quantizer board) for desired minimum pulse width to be passed through the pulse width discriminator. The inhibit pulse can be observed at either pin 4 of the 74123 (Z7) or pin 2 of the 7400 (Z8). Adjust R19 for a pulse width equal to the inhibit pulse width. Observe the pulse at pin 12 of the 74123 (Z7) or pin 12 of the 7400 (Z8).

4.2 COMMON DIGITIZER ADJUSTMENTS.

The common digitizer (CD) timing must be changed to compensate for the 7.2-μs delay of the lumped-constant delay line and for miscellaneous delays in the trigger and video processing circuitry of the stagger/destagger equipment. A coarse timing correction is made with the beacon pretrigger thumbwheels in the National Airspace System (NAS) interface equipment rack. This correction is in 0.1-nmi (approximately 1.2-μs) increments. Final correction is made by restrapping card jumper wires in the CD. A change must also be incorporated in the CD to allow use of an external beacon test trigger (staggered test trigger from the stagger/destagger equipment). The following procedure is included.

Step 1. Set up coarse timing correction using thumbwheels on NAS interface equipment.

Step 2. Rejumper CD card CBFF6 to permit use of an external beacon test trigger.

a. Remove wire strap from 32 to 44.
b. Install wire strap from 32 to 19.

Step 3. Rejumper or install new cards at the following locations to provide final corrections:

Card No.	Function(s)
CBBH6	Map maximum range reset. Memory real time reset. Maximum range.
CBFJ6	Interlace.
BAHEØ	Azimuth preset to accommodate interlace.

5. PHOTOGRAPH AND DRAWINGS.

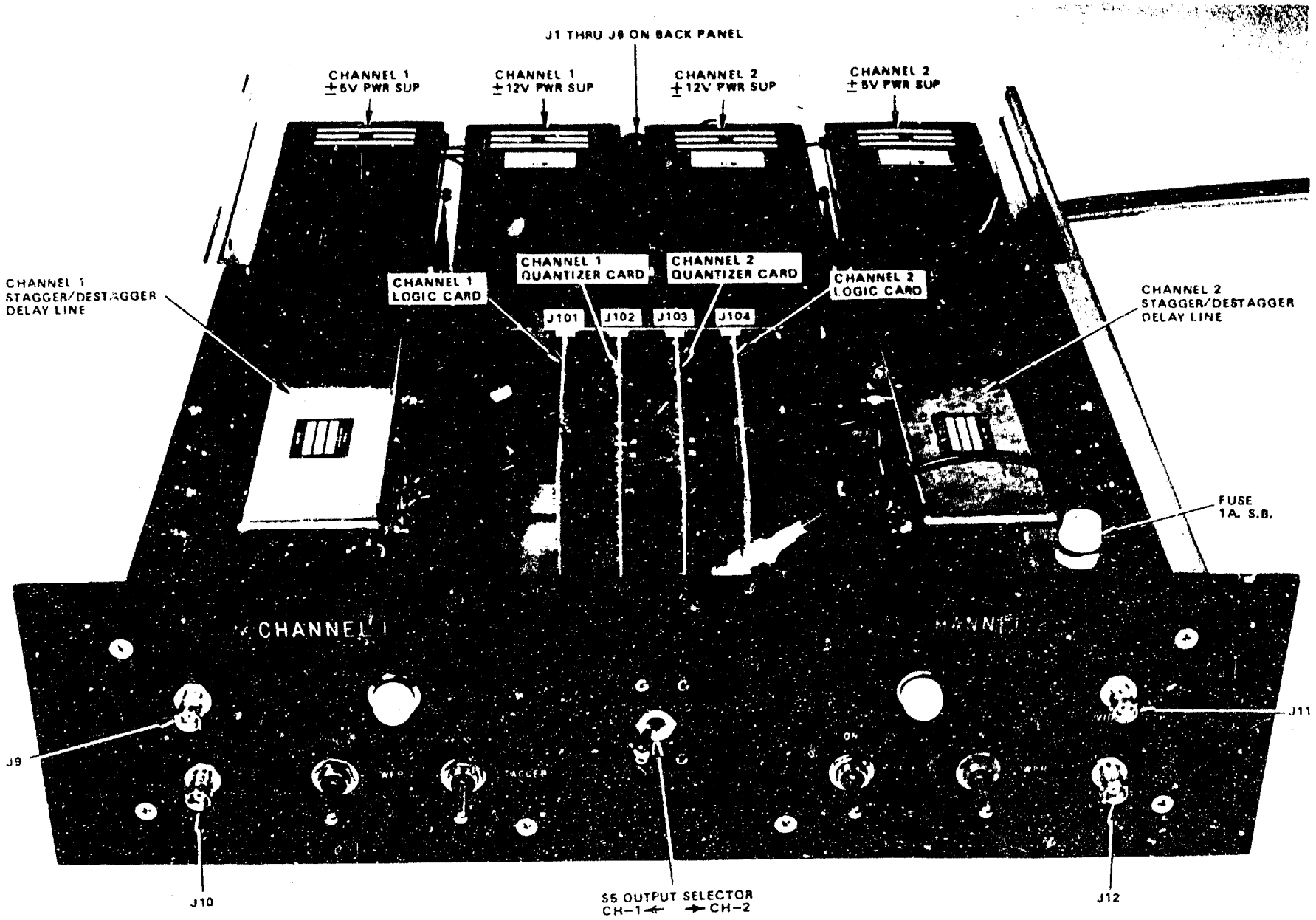
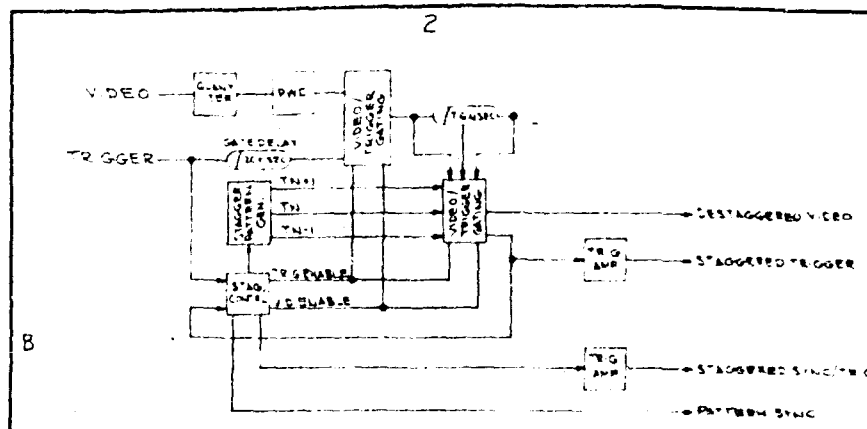
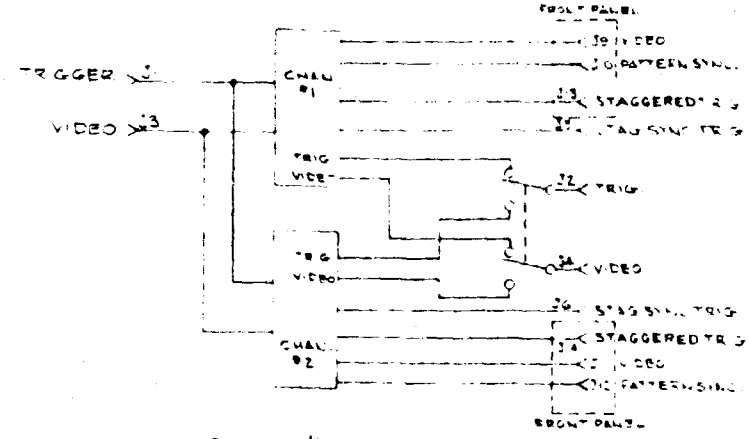


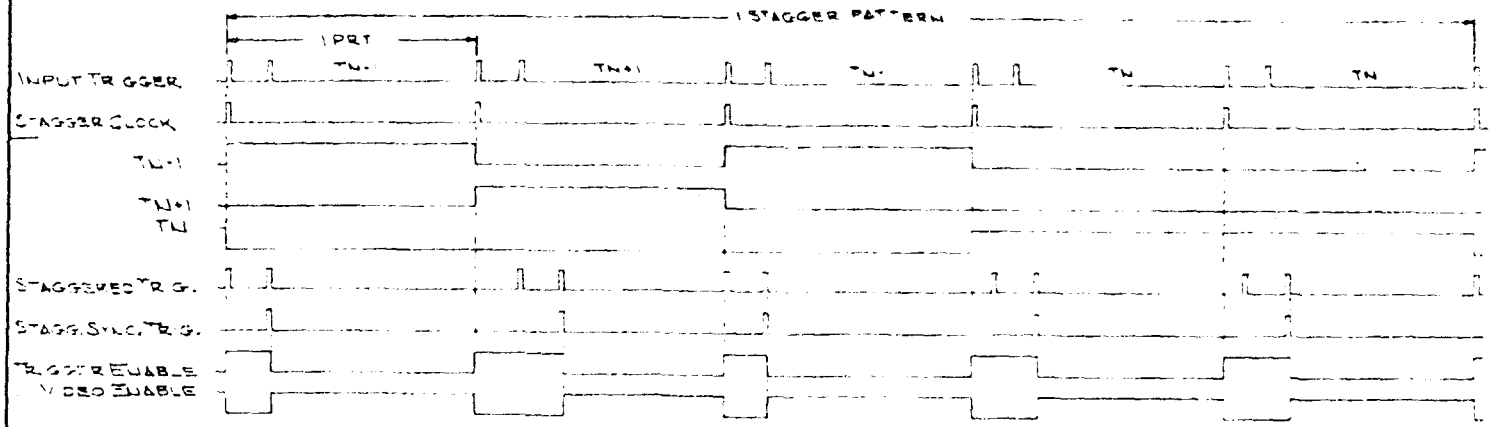
FIGURE 5-1. STACGER/DESTAGGER CHASSIS



STAGGER/DESTAGGER CHANNEL BLOCK DIAGRAM.



STAGGER/DESTAGGER SYSTEM BLOCK DIAGRAM.



STAGGER/DESTAGGER TIMING DIAGRAM.

REVISIONS			
A	4-4-75	ADDITIONS & DELETIONS	

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NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.

STAGGER/DESTAGGER DIAGRAMS.

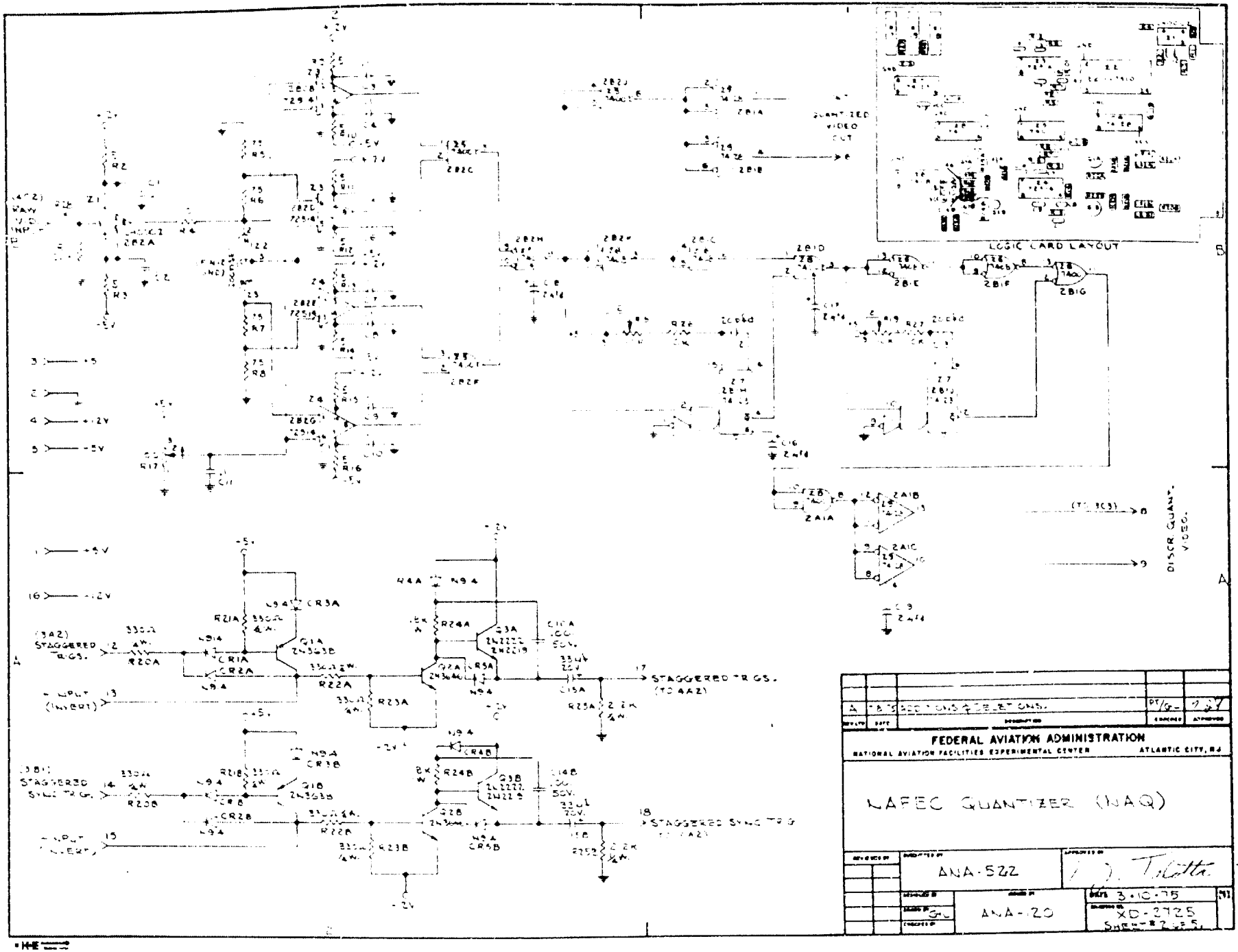
ANA-522

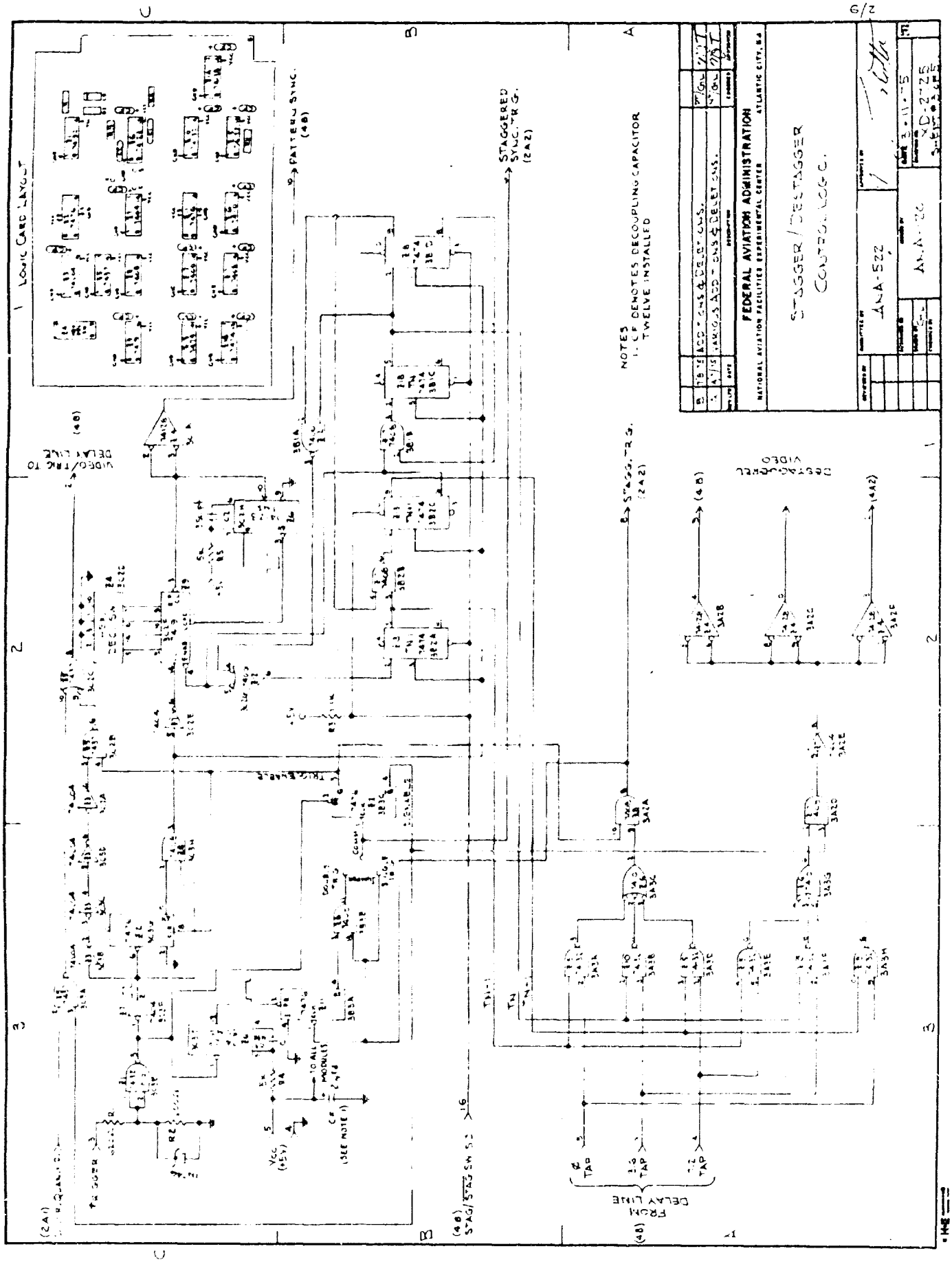
ANA-21

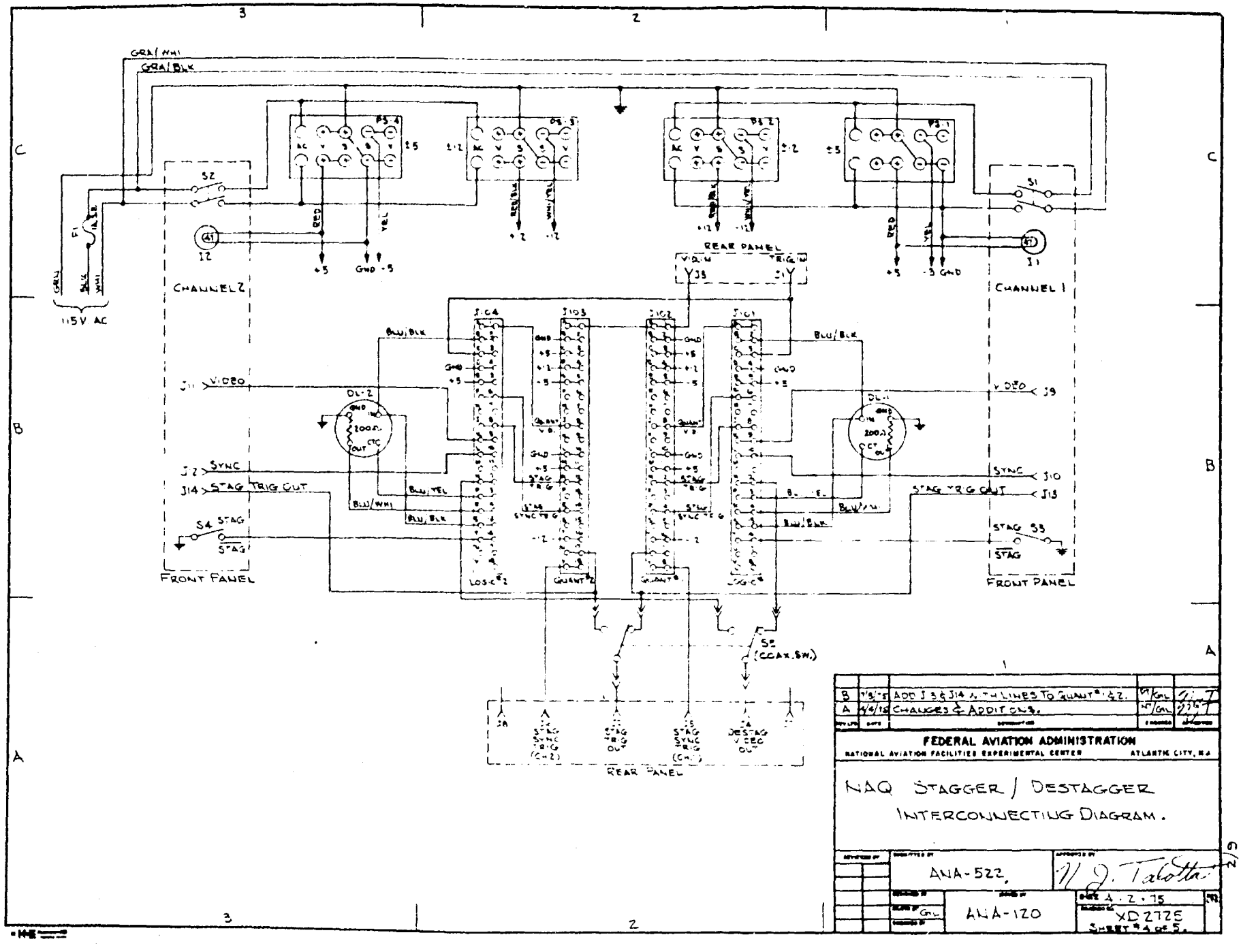
3-7-75

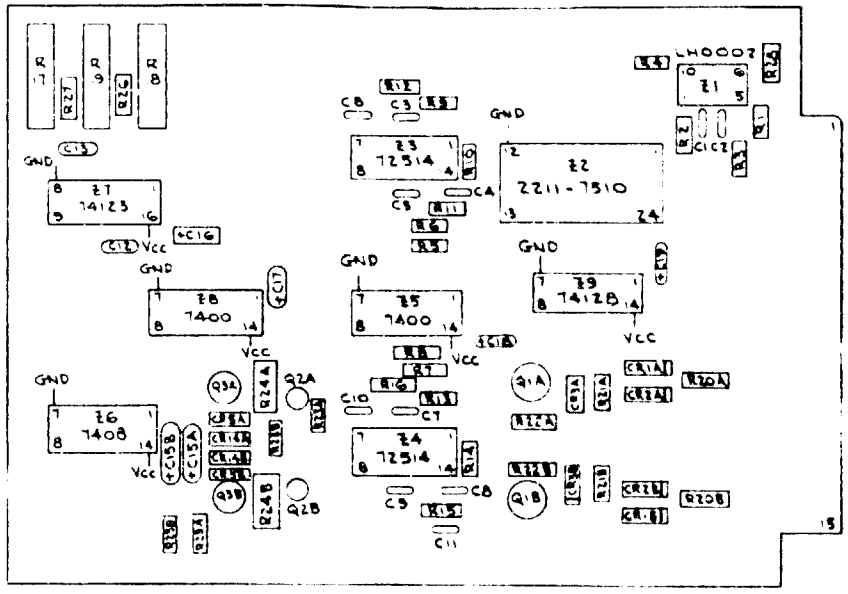
CD-2725

SHEET 1 OF 2

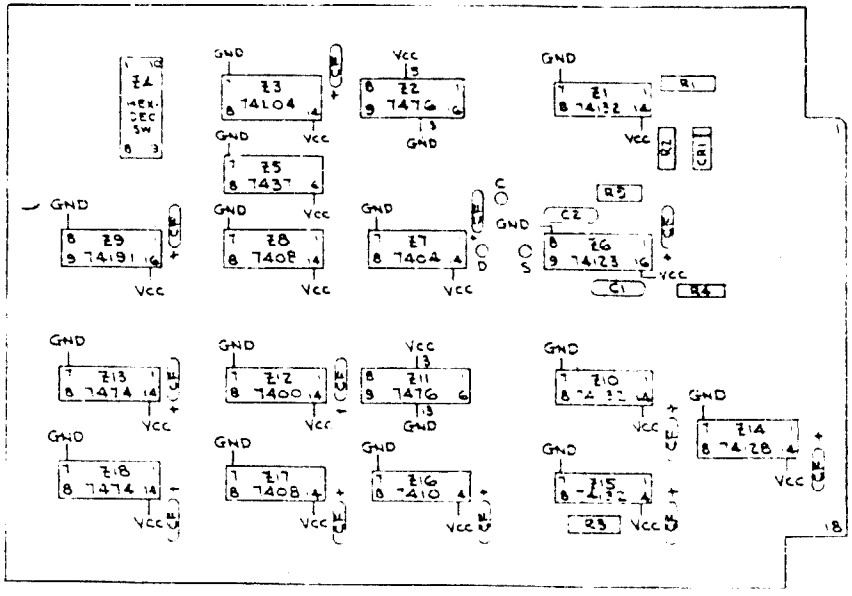

LOGIC CARD LAYOUT
QUANTIZED VIDEO OUT
DISCR QUANT. VIDEO
STAGGERED TRGS. (TO 4AZ)
STAGGERED SYNC TRG.
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, NJ
NAFEC QUANTIZER (NAQ)
ANA-522
ANA-20
XD-2725
3-10-75


FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER
ATLANTIC CITY, N.J.
STAGGER / DESTAGGER
CONTROL LOGIC
ANA-522
NOTES
1. CF DENOTES DECOUPLING CAPACITOR
TWELVE INSTALLED
LOGIC CARD LAYOUT
PATTERN SYNC.
STAGGERED SYNC. TRG.
VIDEO/TRK TO DELAY LINE
DESTAGGERED VIDEO
FROM DELAY LINE


GRN/WHT
GRN/BLK
115V AC
CHANNEL 2
CHANNEL 1
REAR PANEL
FRONT PANEL
FRONT PANEL
REAR PANEL
VIDEO
SYNC
STAG TRIG OUT
STAG
STAG
VIDEO
SYNC
STAG TRG OUT
STAG
STAG
BLU/BLK
BLU/YEL
BLU/WHT
BLU/BLK
S2 (COAX. SW.)
DL-2
DL-1
200Ω
CTC
OUT
RED
YEL
+5
GND
-5
+12
-12
B 7/8/75 ADD J3 & J14 A, TH LINES TO QUANT^R 1&2. GL
A 4/4/75 CHANGES & ADDITIONS. GL
FEDERAL AVIATION ADMINISTRATION
NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER ATLANTIC CITY, N.J.
NAQ STAGGER / DESTAGGER
INTERCONNECTING DIAGRAM.
ANA-522.
ANA-120
A. J. Tabotta
4-2-75
XD 2725
SHEET 4 OF 5



QUANTIZER.



STAGGER/DESTAGGER.

REV LTR	DATE	DESCRIPTION	PT/CH	APPROVED
A	7/8/75	ADDITIONS & DELETIONS	PT/CH	

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NATIONAL AVIATION FACILITIES EXPERIMENTAL CENTER — ATLANTIC CITY, N.J.

PRINTED CIRCUIT CARD LAYOUT.

SUBMITTED BY: ANA-522	APPROVED BY: W. D. Tilotta		
DRAWN BY:	DESIGNED BY: ANA-120	DATE: 4-28-75	SIZE
CHECKED BY:	PROJECT ENGR: G.K.	DRAWING NO: XD-2725 SHEET # 5 of 5	

6/2